Dependable Systems

Faults, errors and failures: Classification and available models

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Most of the material of these slides has been provided by Prof. Cristiana Bolchini, Politecnico di Milano, Italy

TOPIC QUESTIONS

What are the problems we are trying to address?

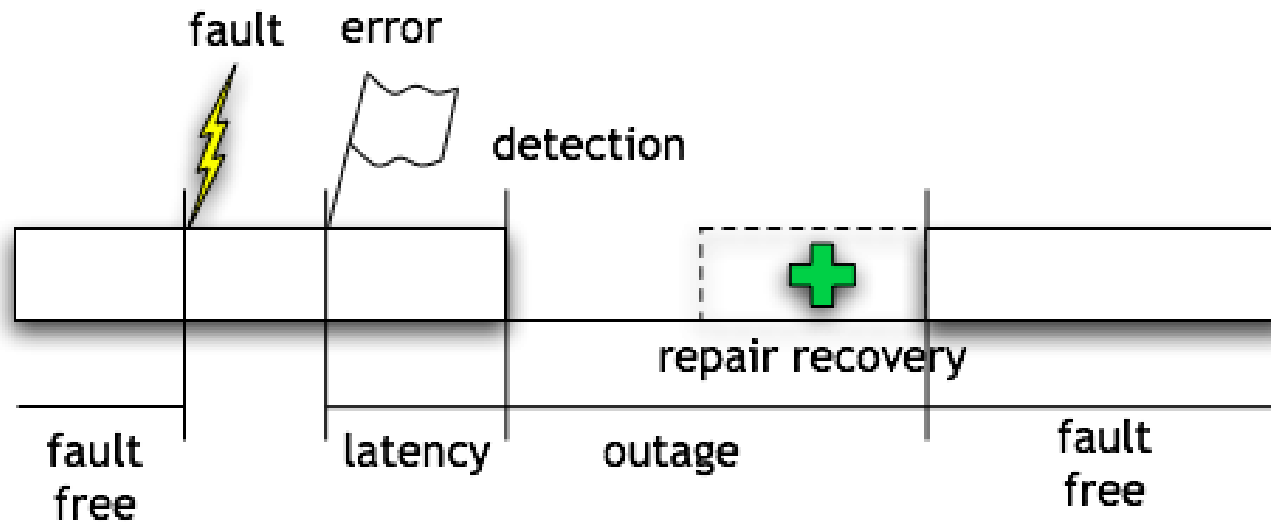
What is the most suitable fault model?

Dependability scenario

- **dependability**
  - problems
    - defect
    - fault
      - permanent/hard (non-recoverable)
      - transient/soft-error (recoverable)
      - recurrent
    - error
    - failure
      - functional
      - timing
    - hazard
    - bug
  - instruments
    - to achieve *design*
      - on-line fault detection
      - fault tolerance
      - autonomous fault recovery
    - to evaluate *analysis*
      - fault coverage
      - system behavior
  - attributes
    - reliability
    - availability
    - safety
    - integrity
    - maintanability
    - testability

Reliability terminology

Term	Description
Fault	A defect within the system
Error	A deviation from the required operation of the system or subsystem
Failure	The system fails to perform its required function



Defects

Non-ideal (non-perfect) fabrication of system components

Examples:

- Thinner/ticker wires
- “Holed” transistors’ gate, source and drain or wires
- …

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Defects are (of course) permanent, but…

…not always defects cause a fault!

Faults

Events that cause a non-ideal (non-perfect) behavior of system components

Examples:

- Stress-induced wire breaks (**permanent fault**)
- Radiation-induced current pulses (**transient fault**)
- Interconnect malfunctions due to specific humidity conditions (**recurrent/intermittent fault**)
- …

Bugs

Non-ideal (non-perfect) source code implementation

Examples:

- Coding errors
- Requirements misinterpretation
- OS, libraries, development tools incomplete support
- …

Defects + Faults + Bugs

Runtime activation may cause errors

Always keep in mind that defects, faults and bugs may stay silent

- They may not affect any component before the triggering condition occurs

We talk bout **fault activation**

Errors

Any unexpected incorrect behavior of a **component/subsystem**

Always keep in mind that also errors may stay silent

- They can be masked in any point between the fault location and the output of the system

We talk bout **error propagation**

Failures

Any unexpected incorrect behavior of the **entire system**

Examples:

- The system produce an incorrect output (**functional failure**)
- The system produce an output (either correct or not) at the wrong time (**timing failure**)

The "bathtub" viewpoint

System failures are due to:

- *Infant mortality*: random production defects, process variation…
- *Normal functioning*: constant random fault occurrence due to the working environment (radiation, heat, humidity…)
- *Wearout*: normal long-term use of the system that cause aging of the materials

The sum of these effects causes all system failures

The “bathtub” viewpoint

Decreasing Failure Rate

Constant Failure Rate

Increasing Failure Rate

Observed Failure Rate

Early *Infant Mortality* Failures

Wearout Failures

Constant (Random) Failures

Failure Rate

Time

Yield

During the production process it is impossible to completely avoid defects (basic cause of faults and errors)

Yield: provides a measure of the amount of functioning devices with respect to the entire production (manufacturing yield)

Faults, errors and failures in
digital circuits and systems

Fabrication defects & functioning faults

Fabrication defects: introduced during component production causing faults, such as:

- Spot defects
- Systematic defects

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- Spot defects
- Systematic defects

Functioning defects: are activated during the functional life of the device because of failure mechanisms, such as

- Gate-oxide break
- Broken contacts
- Wareout effects

Fabrication defects

Spot defects: due to impurities

- Missing material leads to open circuits (dust particles on the masks)
- Extra material leads to short circuits (dust particles on the silicon surface)

Fabrication defects | 2

Spot defects: due to impurities

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- Extra material leads to short circuits (dust particles on the silicon surface)

Systematic defects:
usually occurring in new design processes (e.g. from 65nm to 45nm) solved in time

- Process variation (modifications in the transistors)
- Mask defects

Fabrication defects | 3

CAUSES:

Instabilities in the process conditions

- random fluctuation in the actual environment
- inaccuracies in the control or furnace
- variation in the physical and chemical parameters of the material

Human errors

- Mis-handling of the materials and of the furnace

Fabrication defects | 4

- oxide breakdown
  - formation of pinhole defects due to insufficient oxygen at the interface of silicon (Si) and silicon dioxide (SiO2), chemical contamination, nitride cracking during field oxidation, and crystal defects

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  - formation of pinhole defects due to insufficient oxygen at the interface of silicon (Si) and silicon dioxide (SiO2), chemical contamination, nitride cracking during field oxidation, and crystal defects

Also be due to the operational conditions, e.g., large discharge through the oxide causes local breakdown

Fabrication defects | 5

Vdd

MISSING CONTACT

INPUT B

GATE OXIDE SHORT

INPUT A

OUTPUT

OPEN POLYSILICON

METAL OPEN

METAL SHORT

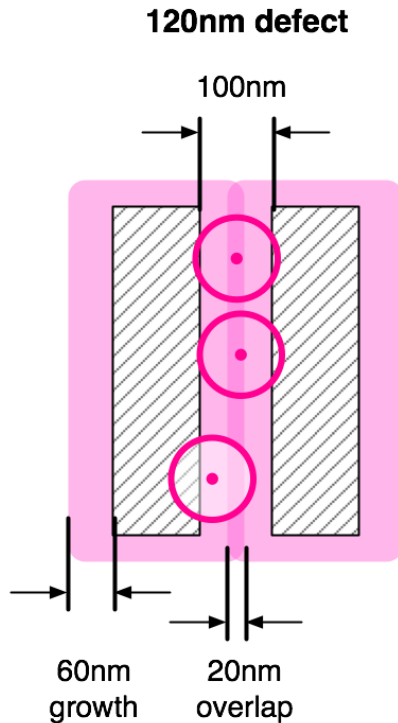
GND

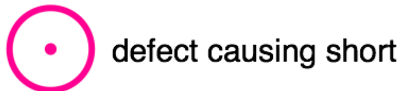
Fabrication defects | 6

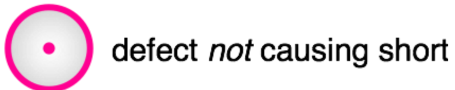
A physical defect causes a fault if its position and size are such to produce an open or short between two lines

Critical Area of a defect – CA
given the diameter x of the defect (which is assumed to be constant and dependent on the technology) CA is the area where a defect has to occur in order to cause a fault

Fabrication defects | extra material | scenario 1







60nm growth around wires

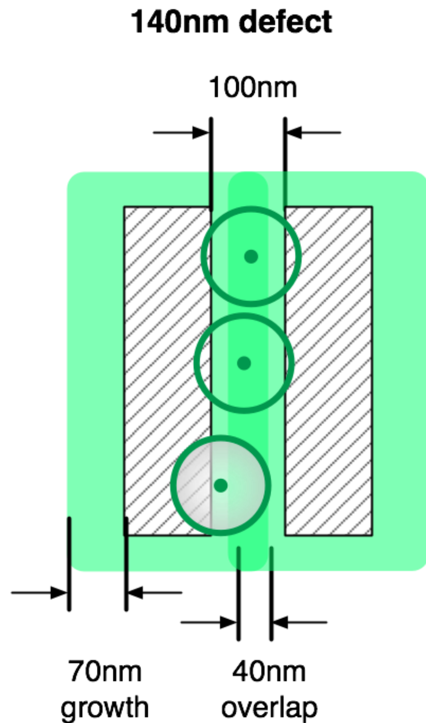
120nm defect

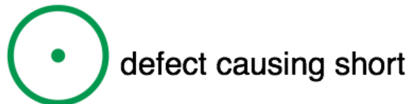
20nm overlap

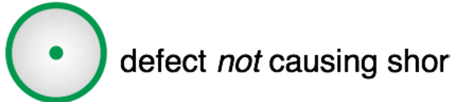
if the center of a 120nm defect falls anywhere in this area, a short between the wires occurs

100nm wires on a 200nm pitch (center-to-center distance)

Fabrication defects | extra material | scenario 2







70nm growth around wires

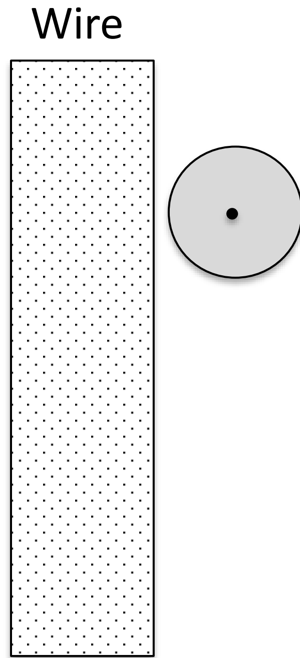
140nm defect

40nm overlap

if the center of a 140nm defect falls anywhere in this area, a short between the wires occurs

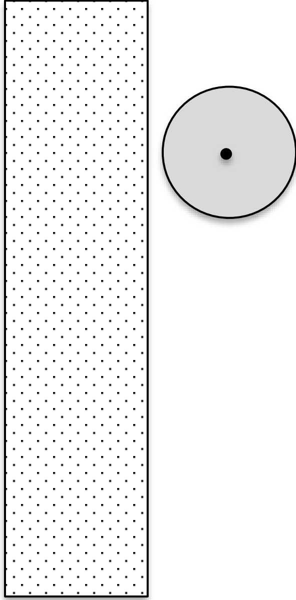
100nm wires on a 200nm pitch (center-to-center distance)

Fabrication defects | missing material | scenario 1



No current flow
interruption

Fabrication defects | missing material | scenario 2



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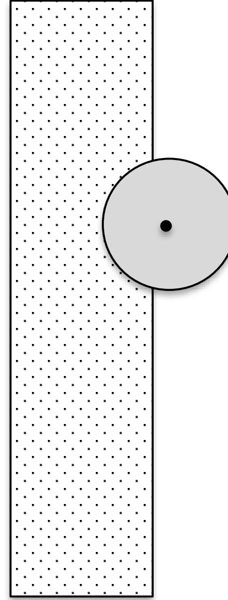
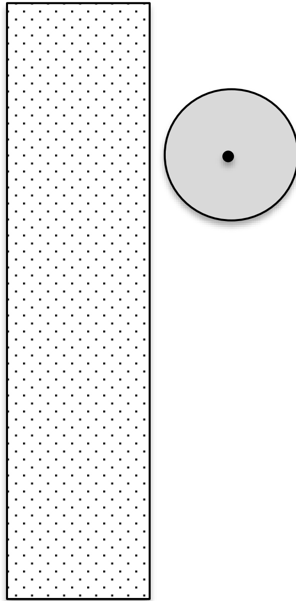
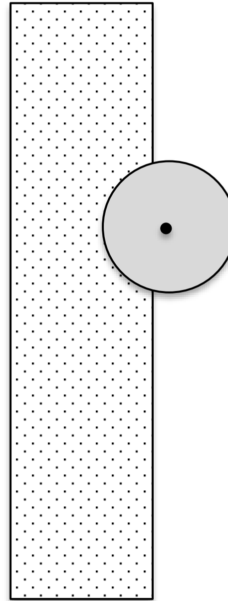
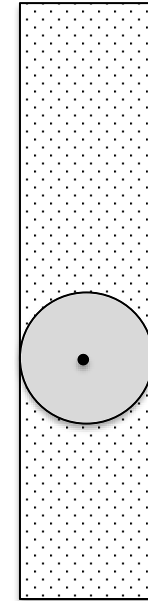


Partial current flow interruption

Fabrication defects | missing material | scenario 3







No current flow interruption

Partial current flow interruption

Complete current flow interruption

Critical areas

Extra material

As defects grow in size, their Critical Areas increase

The rate of the critical area increase is dependent on the spacings in the layout

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Layouts with open spaces are less susceptible to short defects

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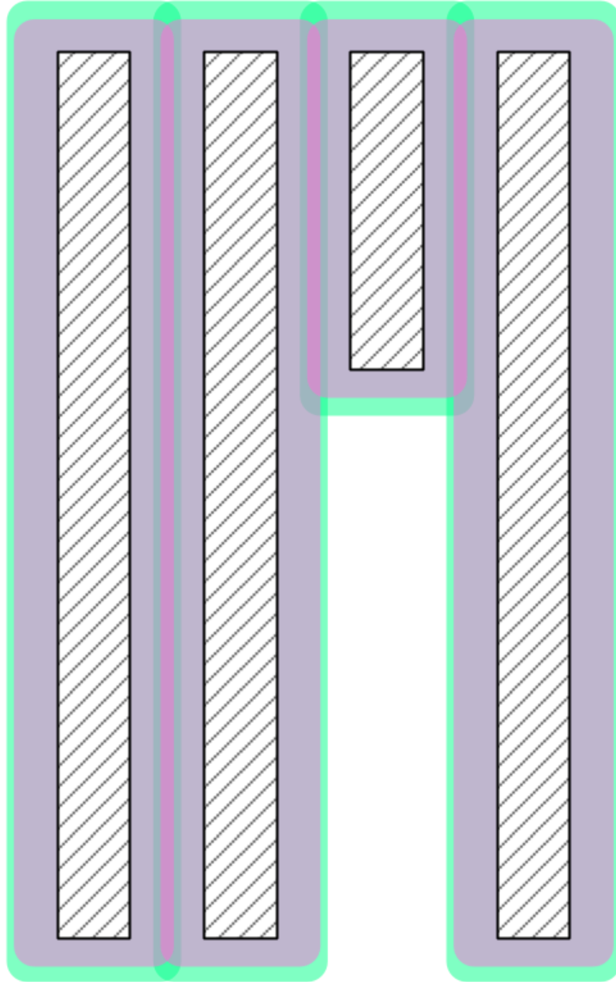
Layouts with open spaces are less susceptible to short defects

Dually, open defects that land on thin wires may more easily halt current flow than open defects that land on thick wires

Critical areas mitigation | wire spreading



Critical areas mitigation | wire spreading

Free area

Critical areas mitigation | wire spreading

Design
modify

Critical areas mitigation | wire spreading

Custom standard cell design done by hand via layout engineers and can

- decrease the critical area for short defects by spreading wires
- decrease the critical area for open defects by widening wires

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The optimum balance, for a given area, depends on the defect density distributions for open defects and short defects…

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The optimum balance, for a given area, depends on the defect density distributions for open defects and short defects…

…and of course on the cost!

Defects and faults

Physical defects

- Fabrication defects (missing or extra material)
- Material degradation over time and/or environment, wear-out

Faults

- A model of the incorrect behavior due to defects

Errors …

Failures …

Abstraction level

Depending on the abstraction level we look these defects at, we may consider different fault models

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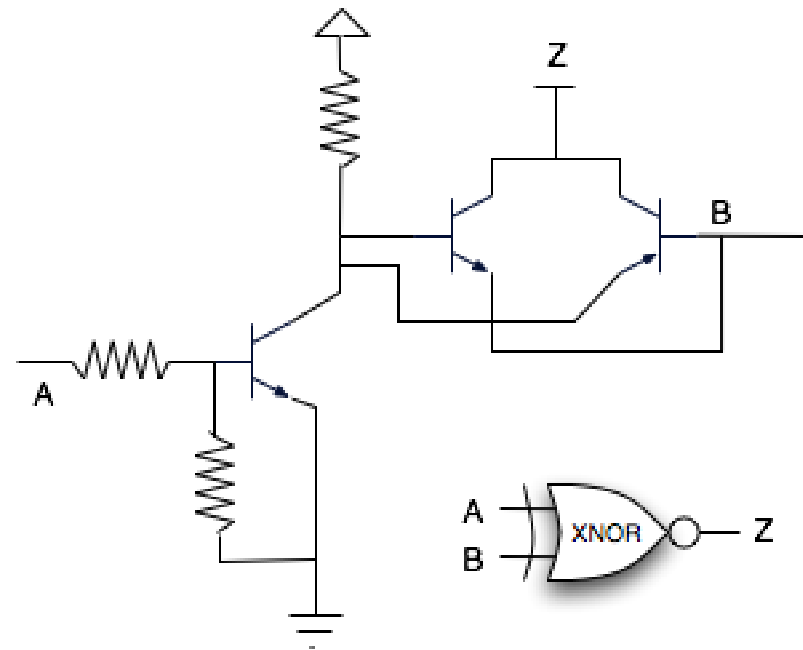
Levels:

- **Transistor**
- Gate
- RTL/Module



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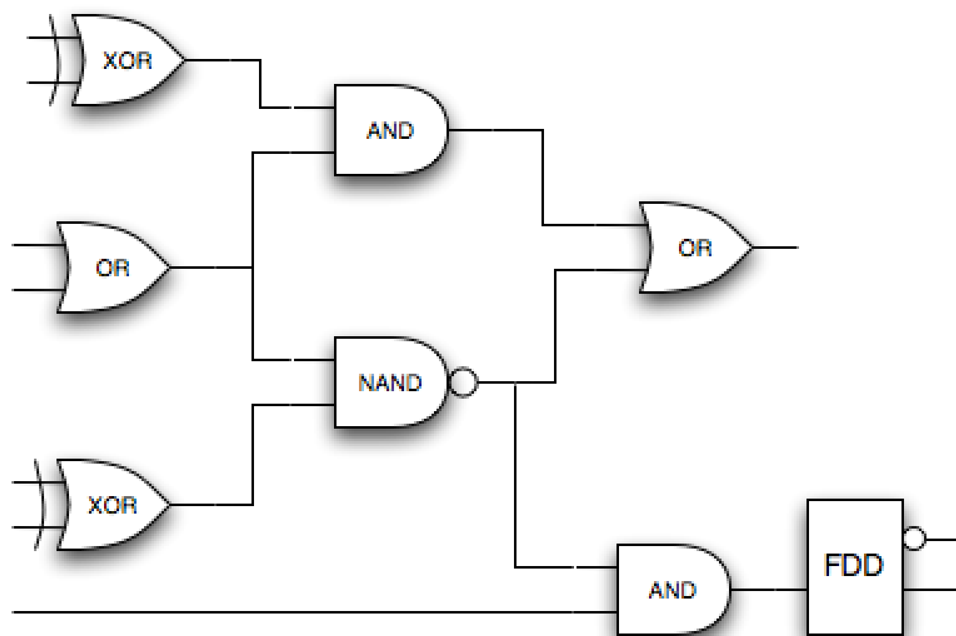

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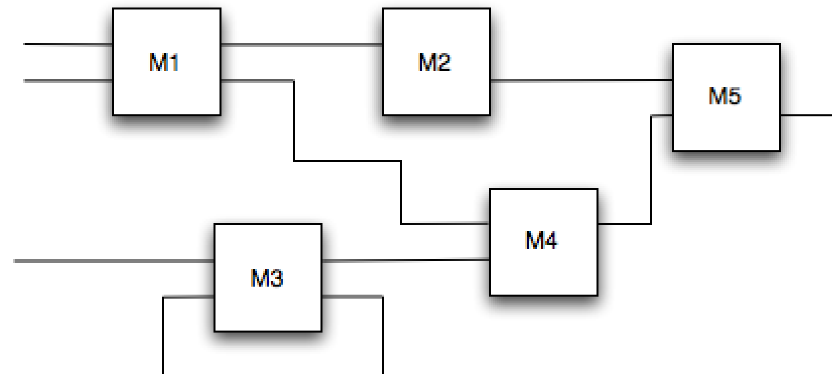

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The lower the considered abstraction level:

- The closer to the device material behavior
- The higher the accuracy
- The longer the analysis time

Different levels of abstraction

BEHAVIORAL VIEW	STRUCTURAL VIEW	
... PC = PC + 1 FETCH(PC) DECODE(PC)	ADD COMP CTRL MEM	ARCHITECTURAL LEVEL
S 0 S 1 S 2 S 3	AN D AN D OR	LOGICAL LEVEL

Fault & time

According to the time duration we classify faults as:

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- **Permanent**: once the fault occurs, it is always there and stable (caused by a defect rather then disturbance)
- **Intermittent**: the fault occasionally occurs (unstable hardware or varying hardware states)
- **Transient**: fault resulting from temporary environment conditions

Fault & time

Testing

- Identification of defects after production/manufacturing (**production test**)
- Periodical health analysis (**on-line self test**)

Fault & time

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- Identification of defects after production/manufacturing (**production test**)
- Periodical health analysis (**on-line self test**)

Fault detection/management/tolerance

- Identification, management and masking of defects and faults occurring during the operational life of the device

Assumptions

When analysing digital circuits/systems these assumptions are considered:

- Single fault or single failure
  - Once a fault occurs, there is enough time to detect it before a second one may occur

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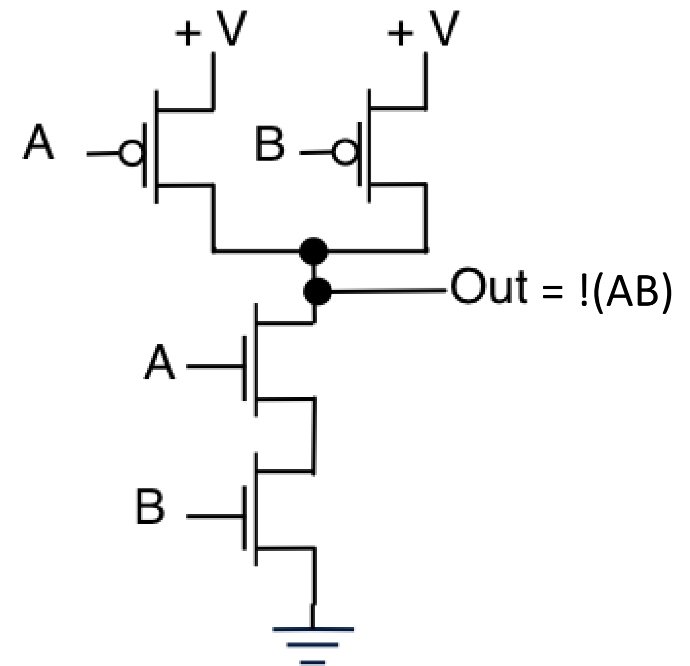
- Single fault or single failure
    - Once a fault occurs, there is enough time to detect it before a second one may occur
- No faults on the primary inputs
    - The input data are always correct

Transistor-level faults

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

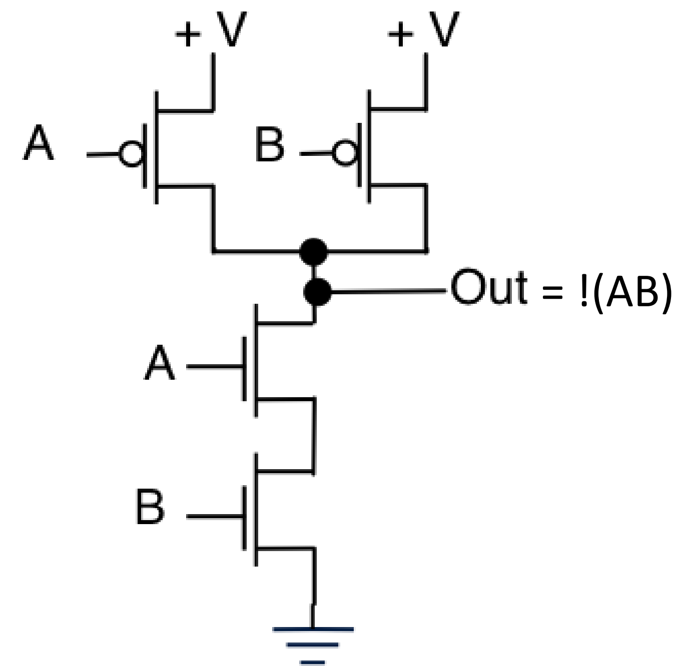


Transistor-level faults

Due to the previously discussed defects a transistor may be:

Transistor Stuck-on (or stuck-short)

- Always connecting



The effect of the fault depends on the affected transistor!

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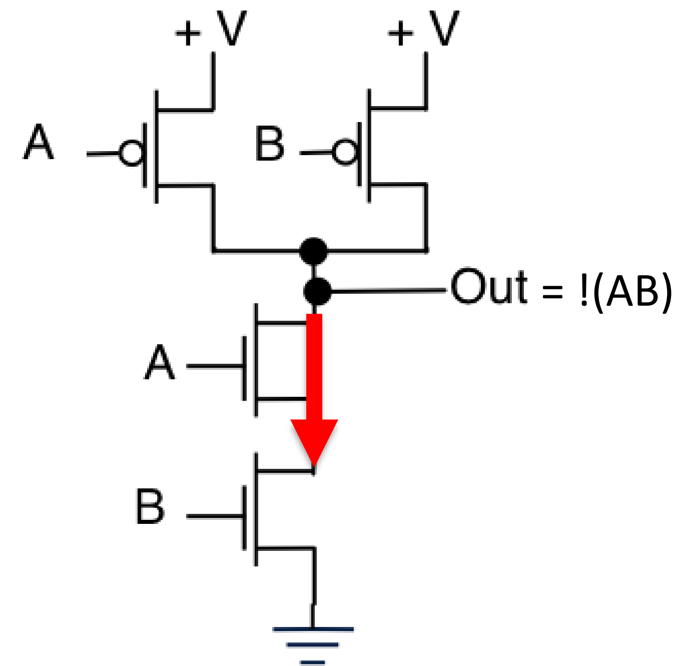

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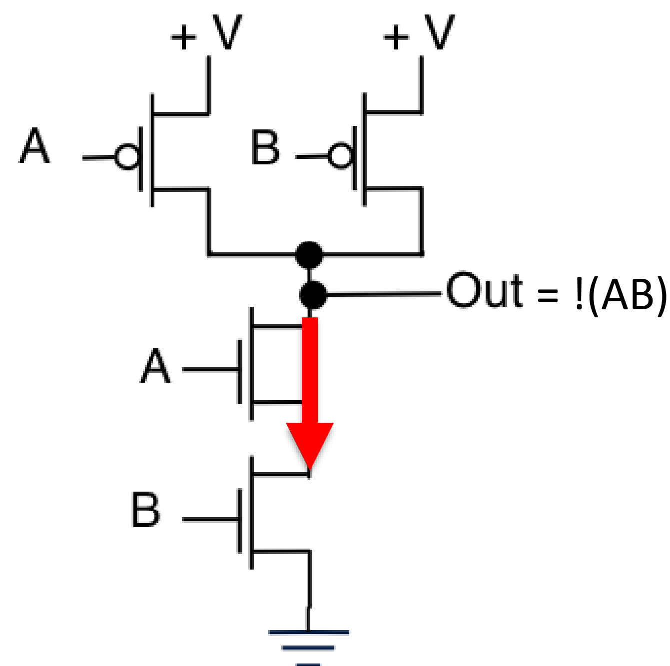

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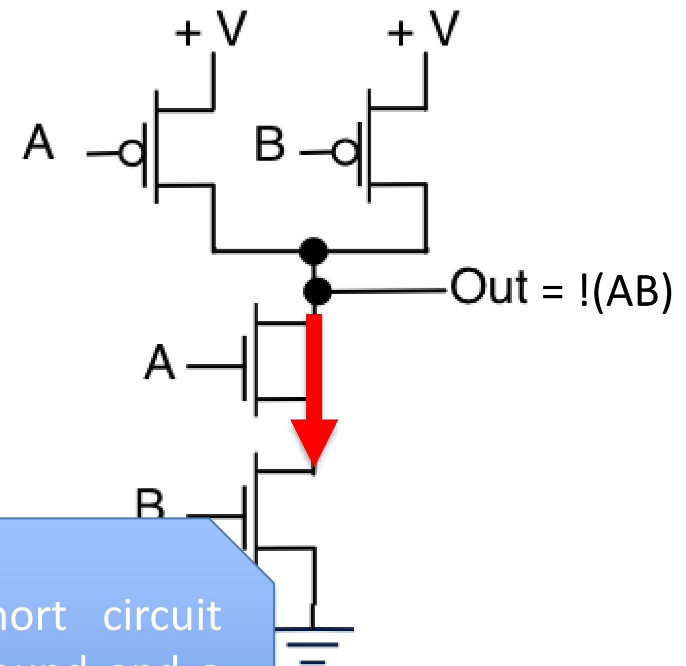

The effect of the fault deper

There will be a short circuit between Vdd and ground and a high current in the gate.

This current can be catastrophic!

Transistor-level faults

Due to the previously discussed defects a transistor may be:

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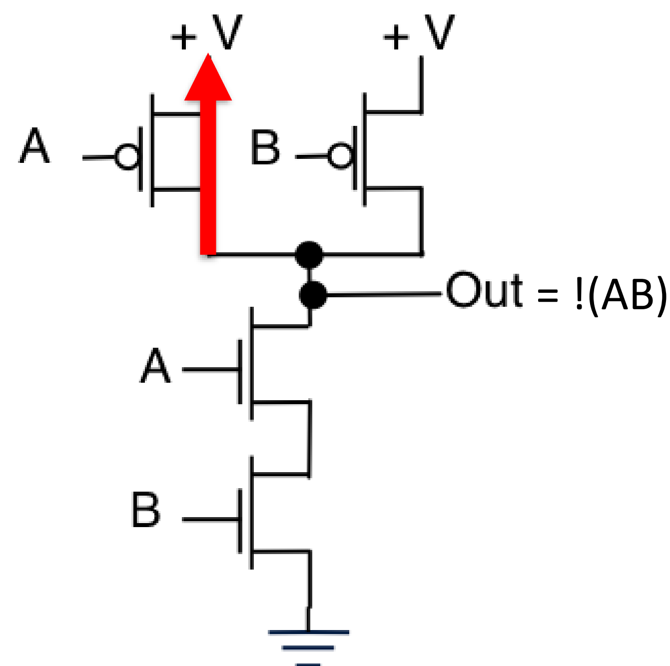
A	B	Out
0	0	1
0	1	1
1	0	1
1	1	?



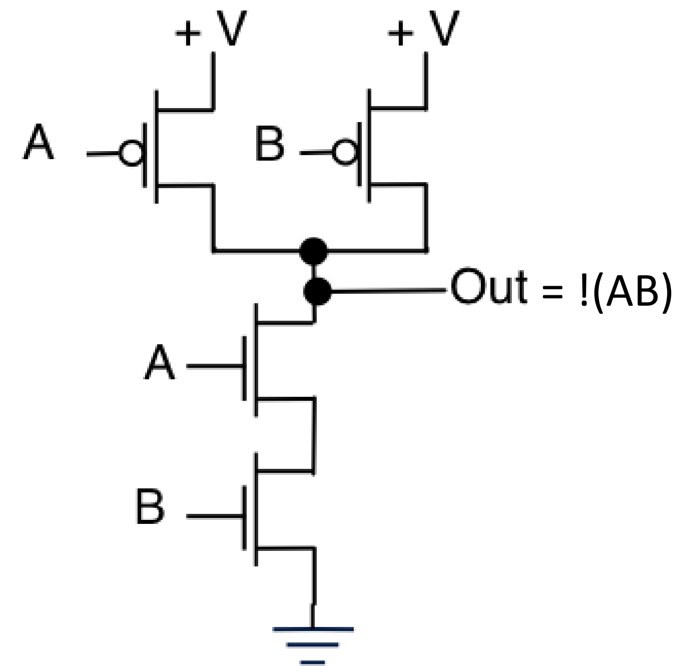
The effect of the fault depends on the affected transistor!

Transistor-level faults

Due to the previously discussed defects a transistor may be:

Transistor Stuck-open

- Always interrupted



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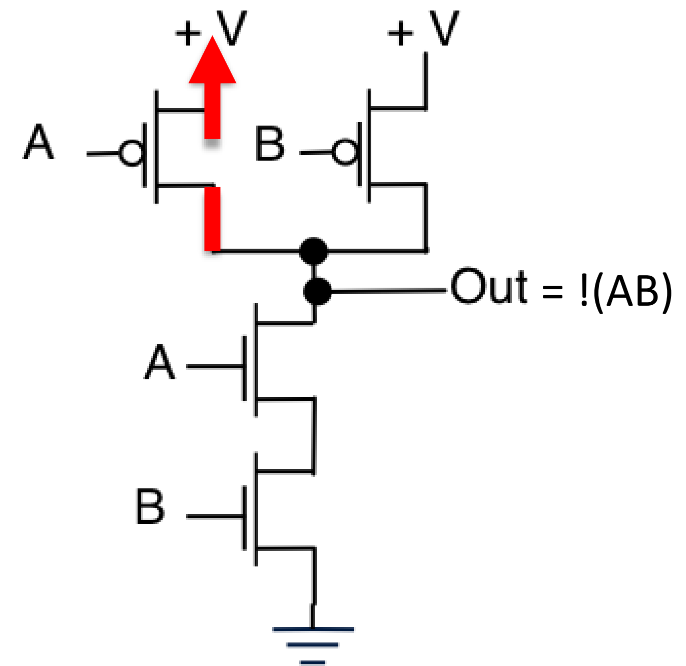

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Transistor-level faults

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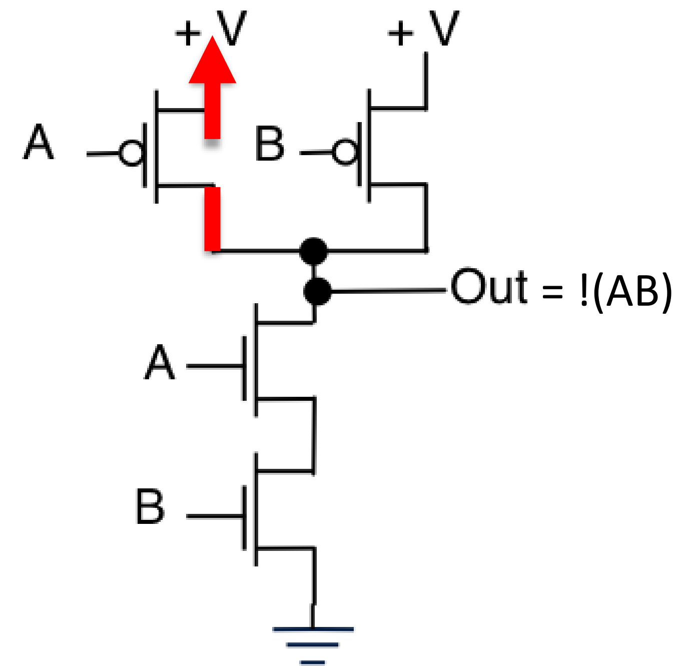
0	1	Z
1	0	1
1	1	0

High impedence



The effect of the fault depends on the affected transistor!

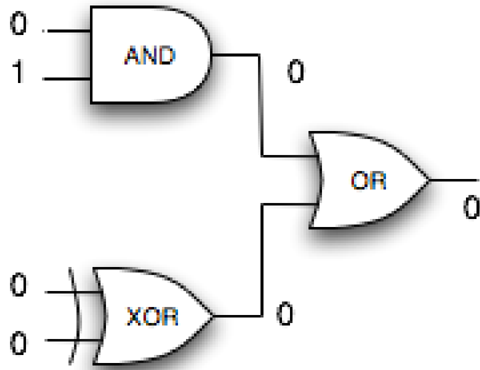
Transistor-level faults

Recap: the stuck- model

- **Stuck-open**: a single transistor is permanently stuck in the open state
- **Stuck-on** (**stuck-short**): a single transistor is permanently shorted irrespective of its gate voltage

Logic level faults

Single Stuck-at Fault (SSF)



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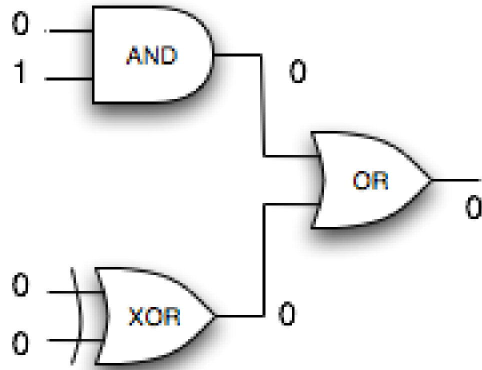

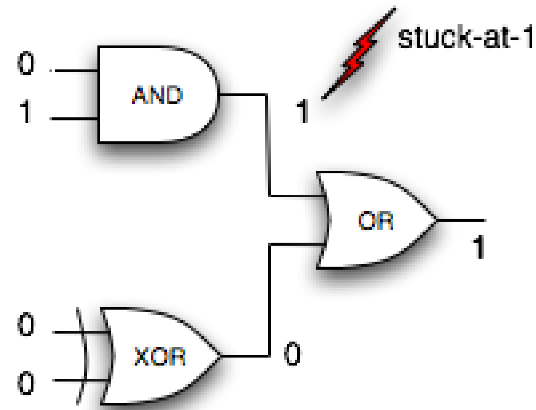

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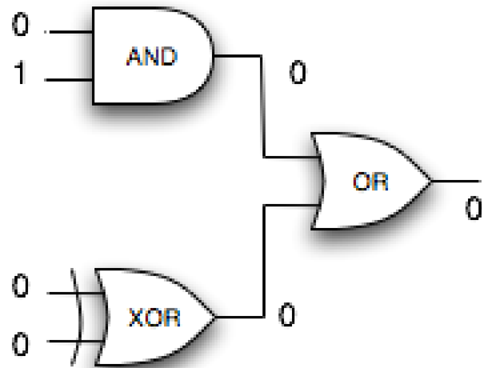
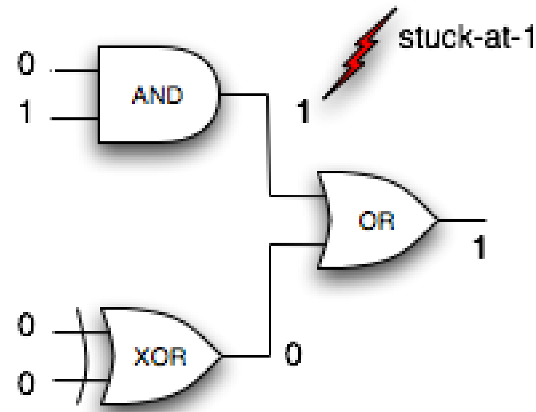
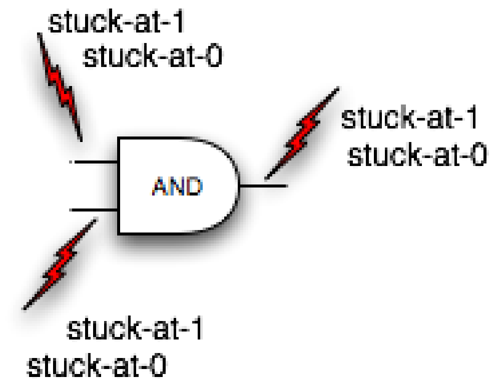




stuck-at-0 and stuck-at-1

- on the gate inputs or output



SSF dictionary

A: SA0 / SA1

B: SA0 / SA1

C: SA0 / SA1

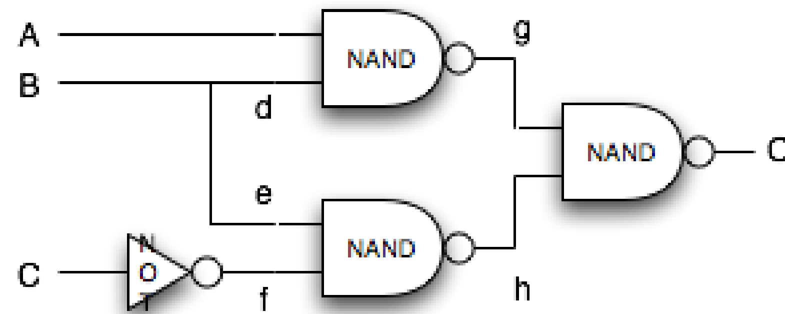
d: SA0 / SA1

e: SA0 / SA1

f: SA0 / SA1

g: SA0 / SA1

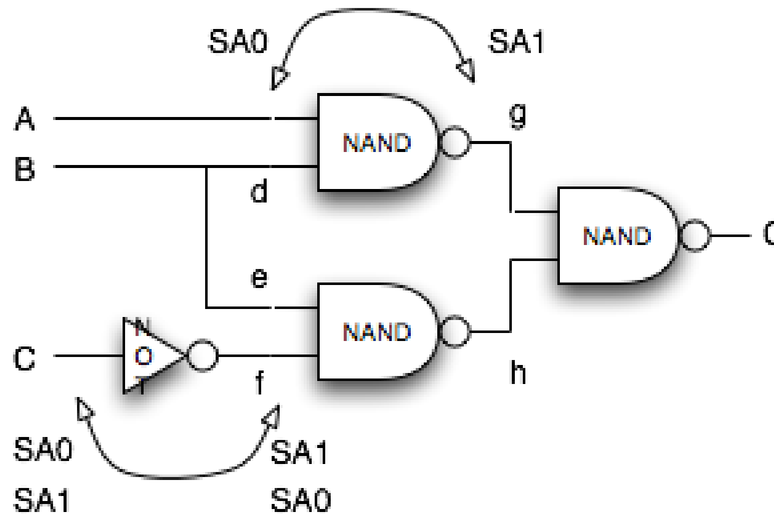
O: SA0 / SA1



Collapsed fault dictionary

Equivalences among stuck-at faults may be identified to reduce the fault dictionary

A: SA0 ≈ d: SA0 ≈ g: SA1



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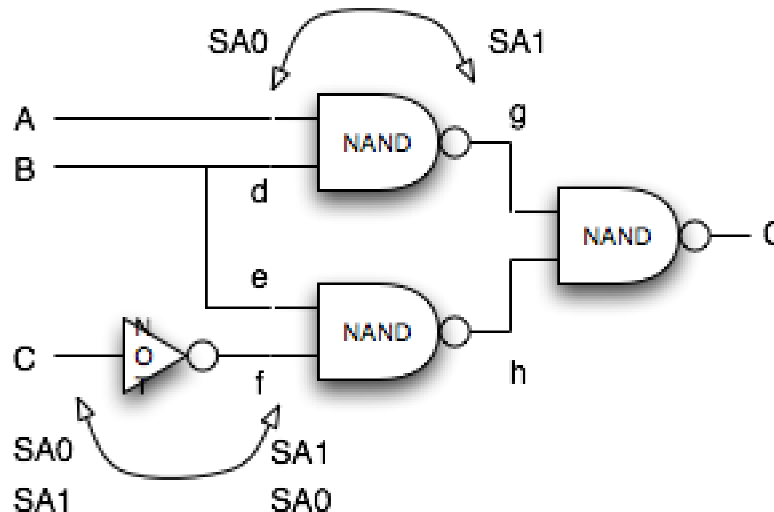

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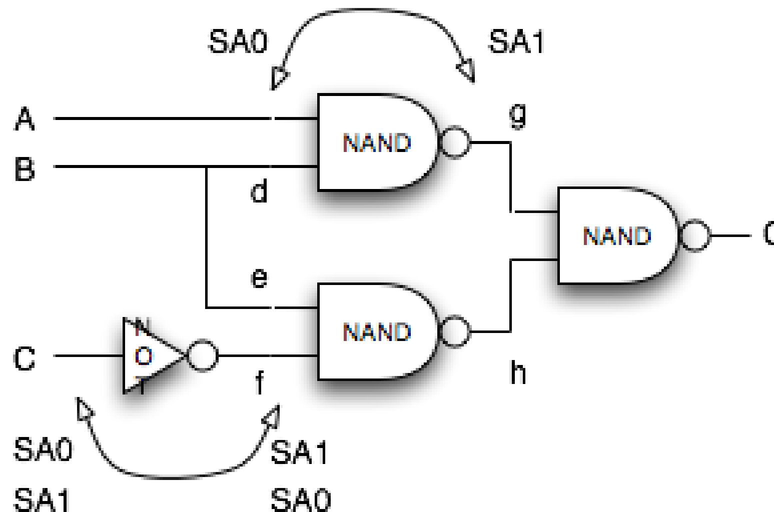
C: SA0 ≈ f: SA1

C: SA1 ≈ f: SA0 ≈ e: SA0 ≈ h: SA1

…



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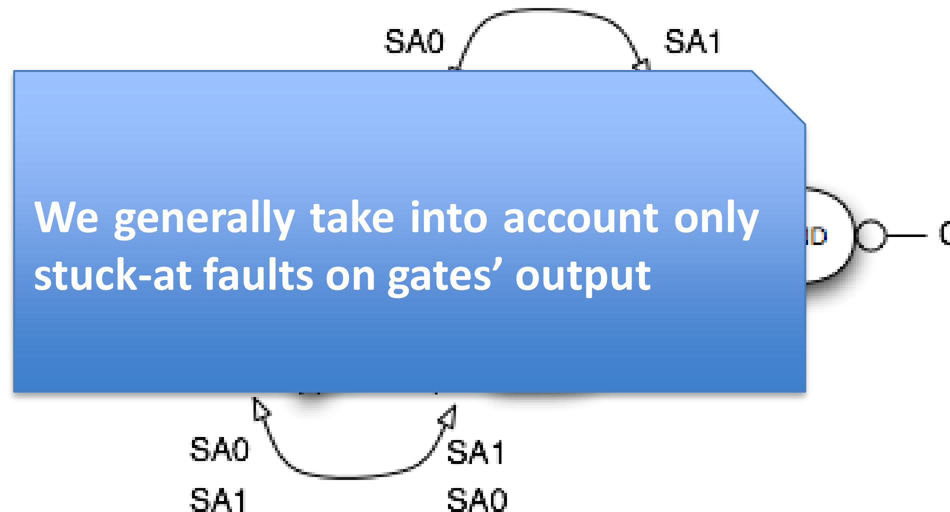
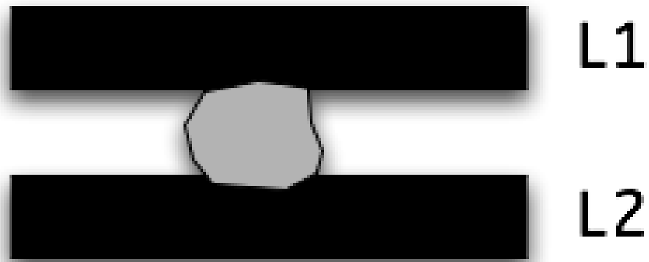


We generally take into account only stuck-at faults on gates' output

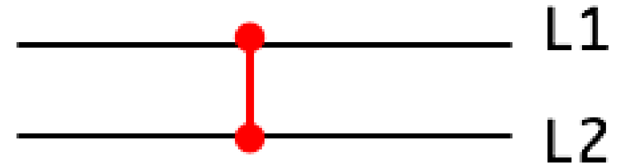
Logic level faults

Undesired connection between two wires:

Physical Defect



Physical Model



Logic level faults

Undesired connection between two wires:

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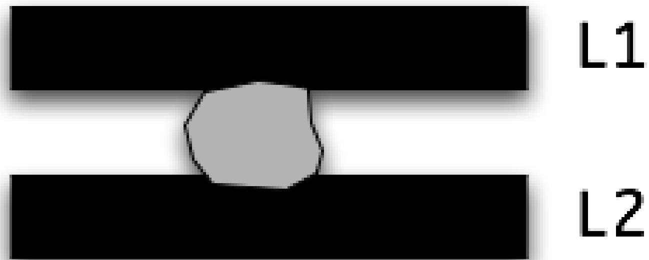
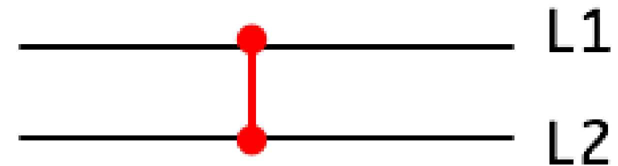
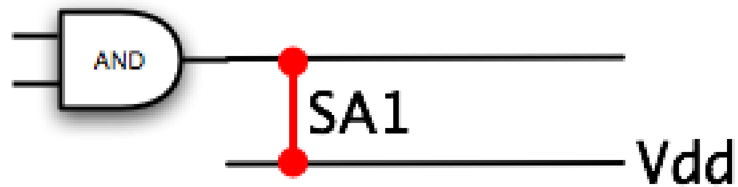


Physical Model



Stuck-at 1

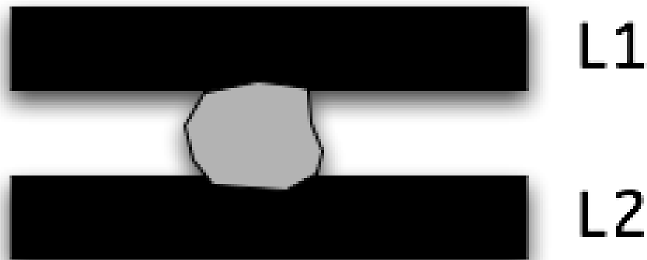


Stuck-at 0

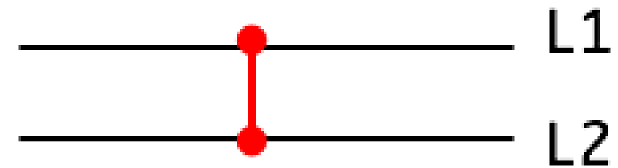
Logic level faults

Undesired connection between two wires:

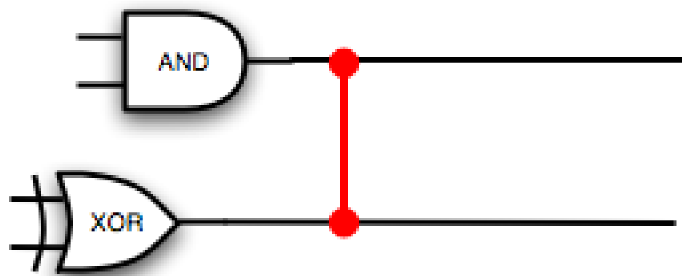
Physical Defect



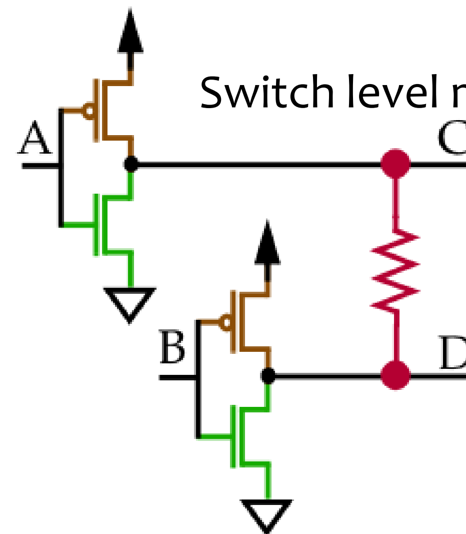
Physical Model



Gate level modeling



Switch level modeling



Bridge fault

Logic level faults

Timing faults: a logic gates produces the right output but with an increased propagation delay

May cause T_{hold} T_{setup} violations of flip-flops!

Radiation induced faults

Ionizing radiations are those with a level of energy able to transfer part of it to the particles they hit

As technology scales, microelectronic devices are more and more sensible to this kind of effects

Types

Single Event Effects - SEE
a measurable effect resulting from the deposition of energy from a single ionizing particle strike

Total Ionizing Dose - TID
a *cumulative* long term ionizing damage mostly due to protons and electrons

Single Event Effects

SEEs can take many forms

- Single Event Transients (SETs)
- Single Event Upsets (SEUs)
  - Bit flips in memory cells
- Multiple Cell Upsets (MCUs)
- Single Event Latchups (SELs), energy from a charged particle leading to an excessive supply power
- Single-Event Functional Interrupt (SEFI)

Classification

Radiation

SEE

TID effect

SEFI

SET SEU MCU SEL

Non-destructive

Destructive

Recoverable

Non-recoverable

Classification

Radiation induced faults

Radiation
SEE
TID effect
soft errors
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Classification

Radiation induced faults

Radiation

SEE

TID effect

soft errors

SEFI

SET

SEU

MCU

SEL

physical degradation

Non-destructive

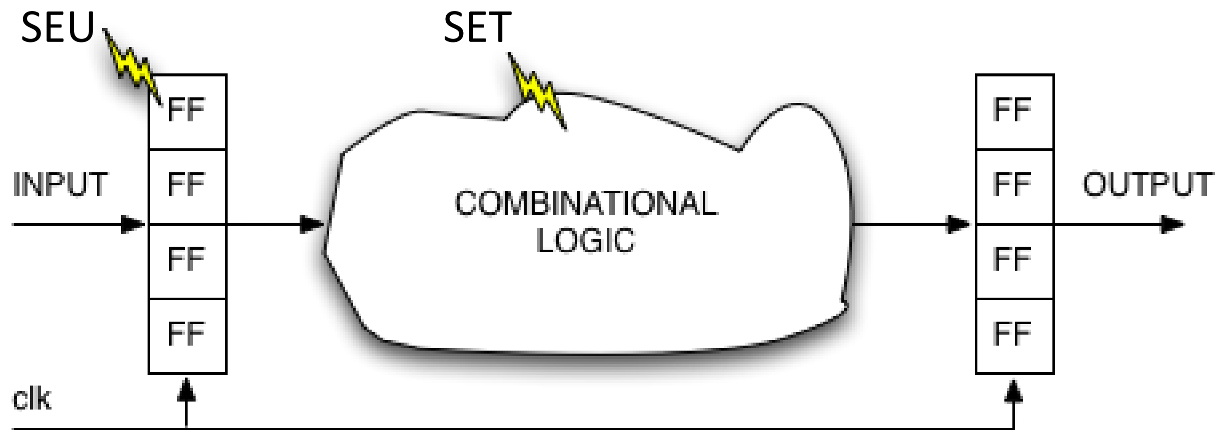
Destructive

Recoverable

Non-recoverable

SETs & SEUs

A single particle hits either sequential or combinational logic

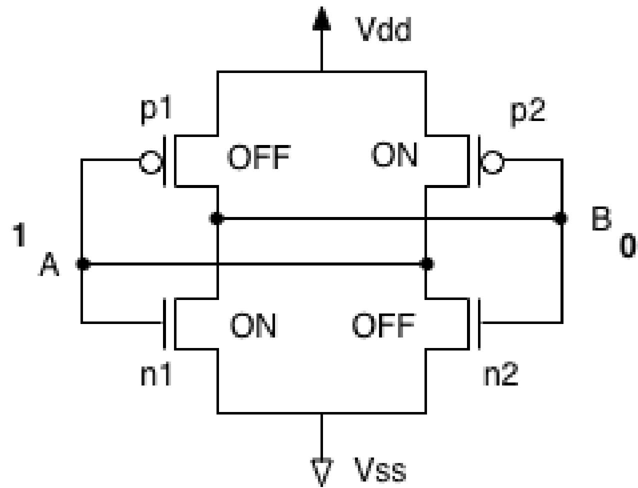


SEUs directly affect memory elements

SETs affect combinational logic, but their effect may propagate to memory elements

SEU in SRAM Memory

Effect: bit-flip



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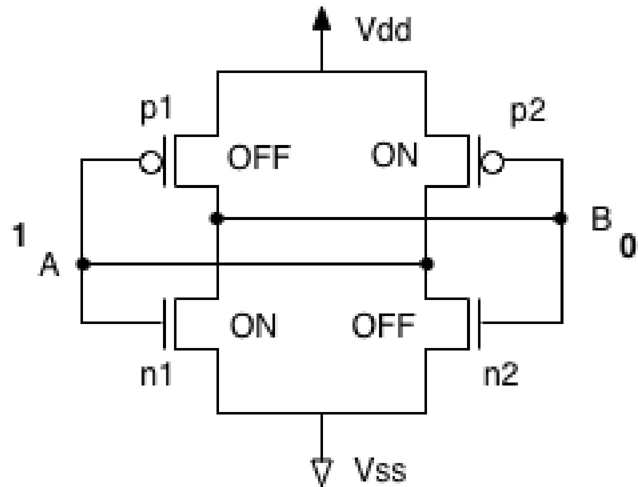

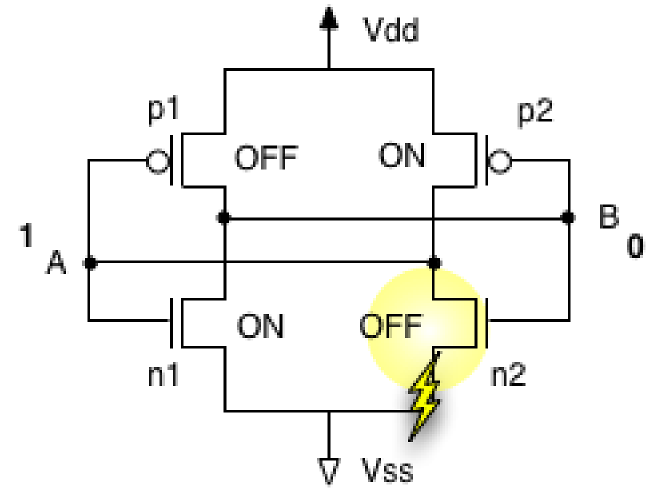

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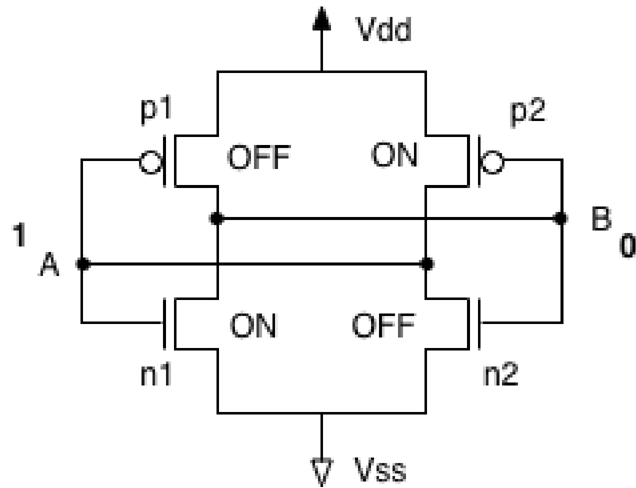
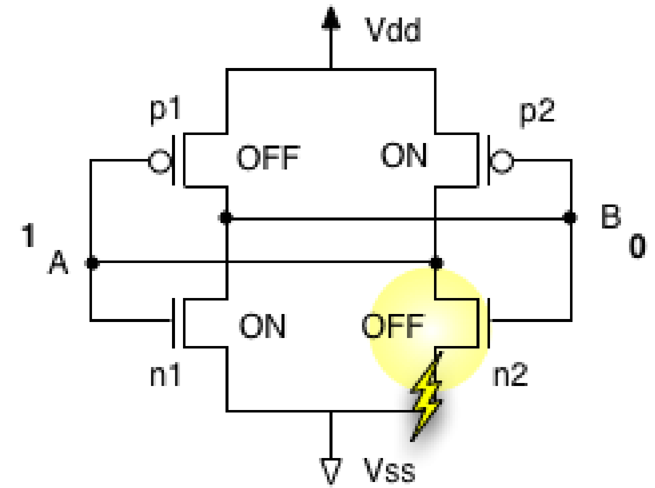
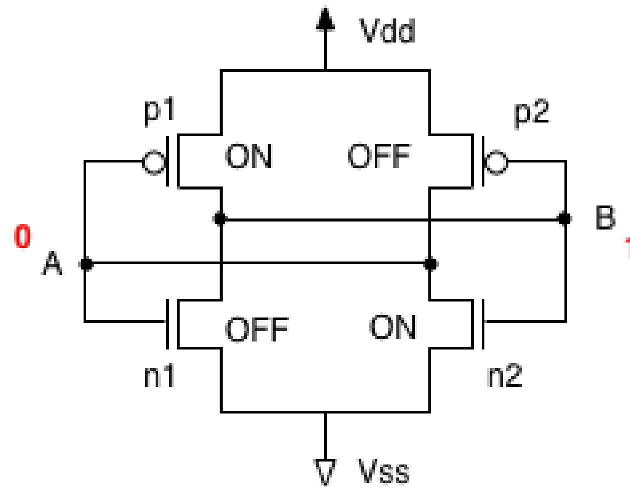






Multiple Bit/Cell Upsets

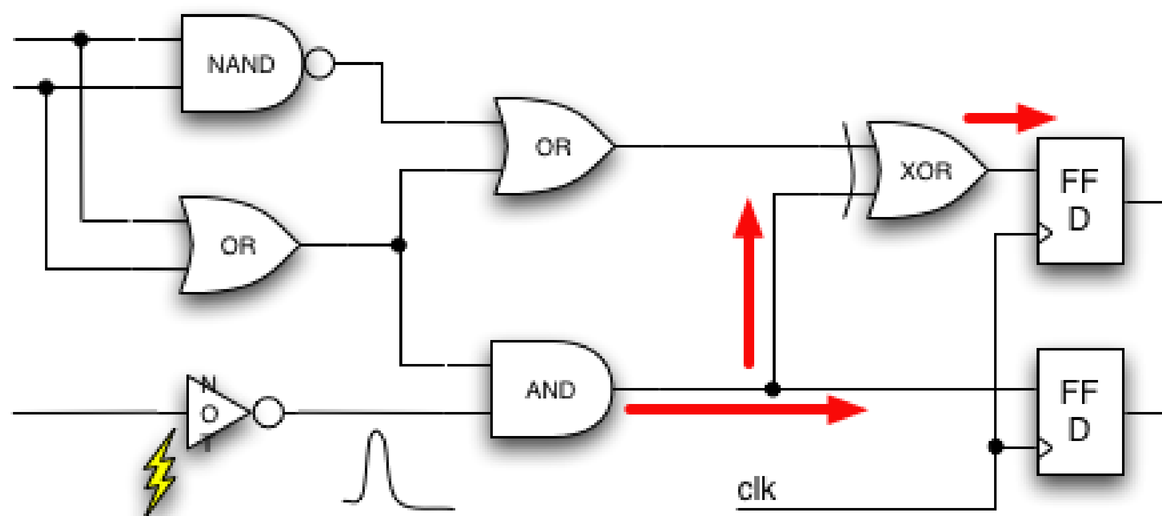
Distributed effect of the radiation, causing more adjacent memory cells to modify their content

Independent SEUs affecting different cells within the design

SET in combinational logic

A transient pulse

- It might get latched or not

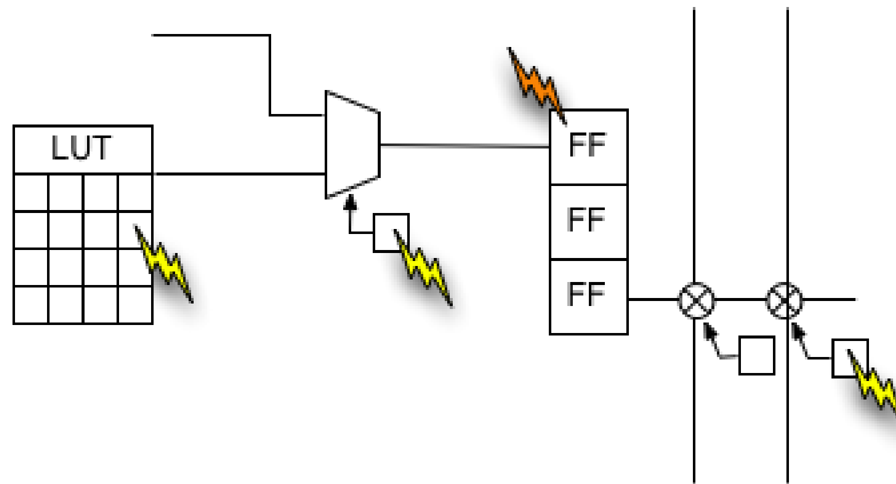


- An erroneous value in the memory element(s)

SEU in SRAM-based FPGAs

Single-Event Upset

- affecting memory elements



SEU in SRAM-based FPGAs

persistent effect

SEU in bitstream

- modifies the functionality of the implemented system
- remains corrupted unless the bitstream is re-written (eventually only partially)

transient effect

SEU in user memory elements

- corrupts the computed data
- a re-execution mitigates the effects

Single-Event Functional Interrupts

Characterizes situations where the event affects a critical signal of the circuit:

- Clock or reset signal
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Recovery:

- Refreshing the corrupted data
- Reloading the altered configuration, and possibly
- Power cycling the circuit

Aging effects

Device degradation due to material stress, environmental harshness, wear-out

Instability at first (intermittent problems, performance degradation …) and permanent faults as the final effect

Main aging effects

- Electromigration – EM
  - occurs in wires and vias as a result of the momentum transfer from electrons to ions that construct the interconnect lattice and leads to hard failures such as opens and shorts in metal lines

Reference: JEDEC Solid State Technology Division

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- Time-Dependent Dielectric Breakdown – TDDB
  - related to the deterioration of the gate oxide layer. Gate current causes defects in the oxide, which eventually form a low-impedance path and cause the transistor to permanently fail
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  - similar to electromigration

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- Stress Migration – SM
  - similar to electromigration
- Thermal Cycling – TC
  - caused by thermal stress due to mismatched coefficients of thermal expansion for adjacent material layers and cause the transistor to permanently fail

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Functional faults | error modeling

The component, core, system has a different behavior with respect to the expected one

- The exact causes are not known because
    - It is not interesting
    - It is impossible
    - It is too expensive
    - …
- The effects are the only thing to work on

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Two important aspects:

- **do not model errors that no fault can generate**
- **model all possible errors that faults can generate**

Cross-layer fault/error models

- Cross-layer reliability analysis is today one of the keywords for the research community
    - Try to combine solutions at different levels of abstraction

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- Need to propagate models from lower to higher levels
  - Abstract the fault model
    - Simplification needed to deal with the complexity of the system when described at higher abstraction levels
  - Find a match between the corresponding fault models at different abstraction levels

Cross-layer fault/error models | 2

Example: faults in the CPU registers and functional errors while running an application

A. Faults at transistor level are erroneous transistors output values
B. Faults at gate level are erroneous gates output values
C. Faults at RTL abstraction level:
    - Erroneous value in CPUs registers (SEU, MCU, stuck-at ..)
D. Functional faults at CPU level are:
    - corruption of the execution of an instruction
    - corruption of a stored value
E. Functional faults at program execution level are:
    - Erroneous execution of workflow
    - Data errors

Cross-layer fault/error models | 2

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Challenge: map the correspondence between A and E (or B and E or C and E) in order to work using E (easier) but still being able to estimate fault coverage, effectiveness of a technique, …

Commonly adopted fault models

Fault model	Description
Transistor Stuck-open	A failure in a pull-up or pull-down transistor in a CMOS causing the device to expose a memory-like behavior
Transistor Stuck-on	A transistor is always conducting
Single Stuck-at Fault (SSA)	Line permanently at logic value 0 or 1
Multiple Stuck-at Fault	Several lines permanently at logic value 0 or 1
Bridging Faults	Two or more independent lines assume the same logic value
Delay Fault	Signal delay on one or more path
SEU	Single Event Upset
MCU	Multiple Cell Upset
Electromigration	Open/Short in metal lines
Time-Dependent Dielectric Breakdown	Transistors stop switching
Stress Migration	Transistors stop switching
Thermal Cycling	Transistors stop switching

defects ➧ faults ➧ errors ➧ faliure

A physical production *defect* may result in a *fault*

A *fault*, when excited, may cause an observable *error*

An error is a difference between the correct behavior and the one caused by the presence of a fault in a subcomponent/subsystem

An *error* propagate to the primary output of the system may cause a *failure*

QUESTIONS

What are the problems we are trying to address?

What is the most suitable fault model?

TOPICS

- Existing fault models at different levels of abstraction
- Time-related characterization of the fault
- Platform-related faults