POLITECNICO
MILANO 1863

# Assignment #3

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Each group will read a paper and prepare a 30minutes presentation highlighting:

- Application scenario
- Target hardware technology
- Considered fault model(s)
- Adopted methodology (fault injection, fault simulation, error simulation)
- Main results
- Applicability of the proposed approach

**I will provide you the papers by email**

# Assignment #3

Group **Zibba** will read:

C. Bernardeschi, L. Cassano, A. Domenici and L. Sterpone, "**ASSESS: A Simulator of Soft Errors in the Configuration Memory of SRAM-Based FPGAs**," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 9, pp. 1342-1355, Sept. 2014, doi: 10.1109/TCAD.2014.2329419.

# Assignment #3

Group **The leading guy** will read:

M. Alderighi *et al*., "**A tool for injecting SEU-like faults into the configuration control mechanism of Xilinx Virtex FPGAs**," *Proceedings 18th IEEE Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston, MA, USA, 2003, pp. 71-78, doi: 10.1109/DFTVS.2003.1250097.

# Assignment #3

Group **gaLoni** will read:

C. Bolchini, L. Cassano, A. Mazzeo and A. Miele, "**Error Modeling for Image Processing Filters accelerated onto SRAM-based FPGAs**," *2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, Napoli, Italy, 2020, pp. 1-6, doi: 10.1109/IOLTS50870.2020.9159746.

# Assignment #3

Group **Gnut** will read:

M. Rebaudengo, M. S. Reorda and M. Violante, "**A new functional fault model for FPGA application-oriented testing**," *17th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings.*, Vancouver, BC, Canada, 2002, pp. 372-380, doi: 10.1109/DFTVS.2002.1173534.