POLITECNICO
MILANO 1863

Assignment #4

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Each group will read a paper and prepare a 30minutes presentation highlighting:

- Application scenario
- Target hardware technology
- Considered fault model(s)
- Adopted methodology (fault injection, fault simulation, error simulation)
- Main results
- Applicability of the proposed approach

I will provide you the papers by email

Assignment #4

Group **Zibba** will read:

C. Bolchini, L. Cassano, A. Miele and M. Biasielli, "**Lightweight Fault Detection and Management for Image Restoration**," *2020 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, Frascati, Italy, 2020, pp. 1-6, doi: 10.1109/DFT50435.2020.9250844.

Assignment #4

Group **The leading guy** will read:

A. Sánchez, L. Entrena and F. Kastensmidt, "**Approximate TMR for selective error mitigation in FPGAs based on testability analysis**," *2018 NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*, Edinburgh, UK, 2018, pp. 112-119, doi: 10.1109/AHS.2018.8541485.

Assignment #4

Group **gaLoni** will read:

S. Pontarelli, M. Ottavi and A. Salsano, "**Error Detection and Correction in Content Addressable Memories**," *2010 IEEE 25th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Kyoto, Japan, 2010, pp. 420-428, doi: 10.1109/DFT.2010.56.

Assignment #4

Group **Gnut** will read:

F. F. d. Santos, M. Brandalero, P. M. Basso, M. Hubner, L. Carro and P. Rech, "**Reduced-Precision DWC for Mixed-Precision GPUs**," *2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, Napoli, Italy, 2020, pp. 1-6, doi: 10.1109/IOLTS50870.2020.9159748