Luca Maria Cassano

Date of birth	May 3, 1985
Citizenship	Italian
Languages	Italian (native), English (fluent), Spanish (fluent), Portuguese (fluent), French (basic), German (elementary)
Current position	Assistant Professor (Ricercatore RTD-A)
Affiliation	Dip. Elettronica, Informazione e Bioingegneria Politecnico di Milano, Piazza L. Da Vinci, 32 - 20133 Milano - Italy
Address	Piazza L. Da Vinci, 32 - 20133 Milano - Italy
Email	`luca.cassano@polimi.it`
Web page	`http://cassano.faculty.polimi.it/`

Main facts

- Winner of the European semi-finals of the 2014 *TTTC's E. J. McCluskey Doctoral Thesis Award* for the best doctoral thesis in the field of electronic test technology and runner-up at the award finals.

- 5 papers in IEEE Transactions journals in the last 4 years (1 paper in the *IEEE Trans. on Computers*, 1 paper in the *IEEE Trans. on Industrial Informatics*, 2 papers in the *IEEE Trans. on Computer Aided Design of Integrated and 1 paper in the* IEEE Trans. on Emerging Topics in Computing. *Circuits and Systems*). In total 12 journal papers, 1 book chapter, 1 tutorial and 22 conference and workshop presentations since the beginning of the academic career, in 2010.
  h-index: 8 ⋄ Total citations: 198 ⋄ Academic age: 8 years (src: Google Scholar, May 2018).
  h-index: 7 ⋄ Total citations: 140 ⋄ Academic age: 8 years (src: Scopus, May 2018).

- Co-Principal investigator of *"OLTRE: On-Line Testing and Healing Permanent Radiation Effects in Reconfigurable Systems"*, a 50,000€ research project funded by the European Space Agency with University of Pisa, Politecnico di Torino and University of Bielefeld (project leader: prof. M. Porrmann). Scientific co-Principal investigator of *"FIND^2: A flexible functional diagnosis framework based on machine-learning technique"*, a 100,000US$ grant from Cisco University Research Program Fund of Silicon Valley Community Foundation (project leader: prof. C. Bolchini).

- BS, MS and Ph.D. from the University of Pisa. Two visiting research periods during the PhD course: the first at the Department of Automation and Informatics of the Politecnico di Torino, Italy (March 2012); the second at the Cognitive Interaction Technology - Center of Excellence (CITEC) of the University of Bielefeld, Germany (April 2012 → September 2012). PostDoc Researcher at Politecnico Di Milano (July 2013 → January 2016). Associate Member of the Technical Staff (AMTS) at Maxim Integrated (February 2017 → September 2017). Currently, Associate Professor (Ricercatore RTD-A) at Politecnico di Milano.

Position and Education

Record of Employment

Sept. 2017 – Ongoing

Assistant Professor (Ricercatore RTD-A) at Politecnico di Milano.

Feb. 2017 – Sept. 2017

Associate Member of the Technical Staff at Maxim Integrated mainly working as a Functional Verification Engineer.

Nov. 2016 – Jan. 2017

Teacher of "Sistemi e Reti" and "Tecnologie e Progettazione di Sistemi Informatici e di Telecomunicazioni" at Istituto Tecnico Tecnologico Paritario "S. Freud".

Nov. 2014 – Jan. 2016

Temporary research assistant at the Dipartimento di Elettronica, Informazione e Bioingegneria of the Politecnico di Milano, Italy, working on "FIND^2: A flexible functional diagnosis framework based on machine-learning techniques".
Advisor: prof. C. Bolchini.

July 2013 – July 2014

Temporary research assistant at the Dipartimento di Elettronica, Informazione e Bioingegneria of the Politecnico di Milano, Italy, working on "Exploiting (historical) test output data to improve functional diagnosis".
Advisor: prof. C. Bolchini.

Mar. 2013 – June 2013

Temporary research assistant at the Istituto di Scienza e Tecnologie dellInformazione A. Faedo of the Consiglio Nazionale delle Ricerche, Pisa, Italy, working on "TRACE-IT - Train Control Enhancement via Information Technology".
Advisor: doc. S. Gnesi.

Education

Jan. 2010 – Dec. 2012

Ph.D. in Information Engineering from the Department of Information Engineering of the University of Pisa, Italy.
Thesis title: *Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs*.
Advisor: prof. C. Bernardeschi.

Jun. 2010

Italian engineering licence (Professional practice examination), University of Pisa.

Sept. 2006 – July 2009

M.Sc. in Computer Engineering from the University of Pisa, Italy.
Thesis title: *Servizi di Sicurezza per Sistemi Publish/Subscribe Applicati a Reti Subacquee*.
Advisor: prof. G. Dini.
Grade: 109/110.

Sept. 2003 – July 2006

B.Sc. in Computer Engineering from the University of Pisa, Italy.
Thesis title: *Sistema di Gestione di Risorse Condivise*.
Advisor: prof. F. Marcelloni.
Grade: 103/110.

Sept. 1998 – July 2003

Scientific high school diploma from Liceo Scientifico F. Bruno, Corigliano Calabro, Italy.
Grade: 100/100.

VISITING EXPERIENCES

Apr. 2012 – Sept. 2012

Cognitive Interaction Technology - Center of Excellence (CITEC) of the University of Bielefeld, Germany.
Topic: Development of communication services for a dynamically reconfigurable satellite payload processing system based on FPGAs.
Supervisor: Prof. M. Porrmann.

Mar. 2012

Department of Automation and Informatics of the Politecnico di Torino, Italy.
Topic: Integration of a high-level model for Single Event Upset (SEU) faults into a SEU simulator for FPGA-based systems developed during the Ph.D. period at the University of Pisa.
Supervisor: Prof. L. Sterpone.

SCHOLARSHIPS AND FUNDING

- Post-Doctoral Scholarship from CNR (March 2013 – June 2013).
- Ph.D. scholarship from the Italian Ministry of University and Research (Jan 2010 – Dec. 2012).

AWARDS

- Winner of the European semi-finals of the 2014 TTTC's E. J. McCluskey Doctoral Thesis Award with the PhD thesis "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs,".
- Runner-up of the Finals of the 2014 TTTC's E. J. McCluskey Doctoral Thesis Award with the PhD thesis "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs,".

Research interests

Luca Maria Cassano's research interests fall into the area of *embedded system design methodologies*, with particular emphasis on the development of innovative Computer Aided Design (CAD) tools to support system designers in dealing with reliability and energy related issues.

More precisely, the main research activity carried out by Luca Maria Cassano is focused on the development of CAD tools for fault simulation, automatic test pattern generation, untestability analysis, functional diagnosis and formal verification of electronic circuits and systems. The main goal is to provide system designers with effective and efficient tools (to be applied as early as possible during the design process) to verify the correctness of the system, to study the behaviour of the system in the presence of faults, and to provide the system with fault detection and diagnosis capabilities. Providing such tools to designers is particularly important when the system is meant to be employed in application fields, such as railways, aerospace and health-care, where a failure may cause severe damages to human operators, to equipment and to the environment.

On the energy side, the research activity is focuses on the development of CAD tools to support the designer in the assessment of the energy feasibility of the system before a prototype is available for on-the-field analysis. Such tools are vital when the system under design is a very-low-power device with no energy harvesting capabilities, as in the case of wireless sensor networks (WSNs), and when the system is meant to be employed in harsh environments, such as Antarctic, deserts and high mountains, where post-deployment maintenance is either very difficult and expensive or even impossible, as in the case of automatic weather stations (AWSs).

RELIABILITY-RELATED ISSUES

The main research activities carried out by Luca Maria Cassano focuses on the analysis and test of the effects of Single Event Upset (SEU) faults in the configuration memory of SRAM-based FPGA systems (investigated during the Ph.D. period at the University of Pisa) and on the adaptive incremental functional fault diagnosis at the board-level (tackled during the PostDoc period at the Politecnico di Milano). In both cases, the interest is in using formal methods (stochastic Petri nets and model checking) and machine learning techniques (data mining, decision trees, genetic algorithms and artificial neural networks) in the field of embedded systems reliability.

Moreover, Luca Maria Cassano also started several scientific collaborations outside the above-mentioned research topics, investigating other reliability-related issues.

SRAM-based FPGAs

In the last years, SRAM-based FPGA devices have been more and more employed in safety-critical application fields, and for this reason it is vital to provide designers of such systems with effective tools to analyse the reliability of the system, as well as to test whether the system is affected by faults or not. On the other hand, when this research activity was carried out (2010 $\rightarrow$ 2014) the analysis of the reliability of SRAM-based systems was performed with CAD tools that were originally designed for ASIC systems. These CAD tools were not able to capture all the technological features of the FPGA technology and thus they could hardly be adapted to the analysis of FPGA systems. The main novelty is the design and development of a set of analysis tools that adopted a different fault model than the stuck-at fault model (that is typically considered for digital circuits). The considered fault model has been demonstrated to be much more accurate than the classical stuck-at fault model when the focus is on SEU faults affecting the configuration memory of FPGA devices. An additional novelty of the research was that the engine of the designed tools relied on formal methods (such as stochastic Petri nets and model checking). A summary of the research activity carried out in the field of reliability analysis and test of SRAM-based FPGA systems has been published in [IC.6] and [IC.13]. More in details, the activities carried out in this field are:

- the design, development and experimental validation (through the use of a fault injection board) of ASSESS: an accurate SEU simulation environment based on the stochastic Petri nets formalism. ASSESS has been used to estimate the SEU sensitivity of SRAM-based FPGA systems as well as to assess the fault coverage achieved by externally generated test patterns for fault detection. Publications: [JR.9] [IC.16] [IC.18] [IC.20] [IC.21].

- the design and development of GABES: an environment for automatic test pattern generation addressing SEUs in the configuration memory of FPGA systems. More in details, the approach addressed the configuration bits actually used by the design (application-dependent testing) and it relied on a genetic algorithm for the generation of the test patterns and on the previously developed SEU simulator for the evaluation of the fault coverage achieved by the test patterns. Publications: [JR.11] [WS.8].

- the design and development of a tool for the analysis of the testability of SEUs in the configuration memory used by an FPGA-based system. The designed tool relied on model-checking (the SAL formal specification language and model-checker) and aimed at identifying the configuration bits that could be demonstrated to be formally untestable. The output of this tool has then been used to speed-up the test pattern generation process carried out by the previously designed GABES environment. Publications: [IC.14] [IC.17].

Furthermore, a survey of design issues related to the use of SRAM-based FPGA devices in safety-critical systems has been published in [JR.6].

Board-level diagnosis

In the last years, big effort has been devoted to improve the board-level fault diagnosis process. Much work has been done to exploit historic log of previously performed testing activities to build an accurate model of the board and its components and of the available tests. On the other hand, very few work has been done to actually drive the runtime diagnosis process. The research activity focuses on the design of efficient CAD tools meant to support design/test engineers during the runtime diagnosis process. This research aims at exploiting statistical and machine learning-based techniques (mainly decision trees and data mining) to drive the runtime diagnosis process by determining an efficient test execution order and by identifying the faulty component(s) as early as possible. The final goal is to reduce the number of tests needed to be executed (and thus reduce the diagnosis time and cost) to determine the faulty component(s) on the board by executing tests in an *incremental* and *adaptive* way. More in details, incremental test execution means that after the execution of each test the CAD tool decides whether to execute more tests or to stop the diagnosis process and determine the faulty component; adaptive test execution means that the CAD tools adapts the test execution order based on the outcomes of the previously executed tests. Publications: [JR.4] [JR.7] [TU.1] [IC.2] [IC.5] [WS.1].

Other works

Luca Maria Cassano has been also involved in the following research activities:

- The design, verification and reliability analysis of the safety-critical logic driver of a battery management system for Li-ion batteries. Publications: [JR.10] [IC.11].

- The design of a technique for on-line on-demand self-testing and self-healing for reconfigurable systems. Publications: [IC.4] [IC.8] [IC.15] [WS.6] [WS.7].

- The design and development of a CAD tool for an early analysis of the untestability of stuck-at faults in VLSI systems based on the use of model-checking. Publications: [IC.7].

- The design of an adaptive fault-tolerant flip-flop architecture. Publications: [IC.9].

- The design of techniques for the detection of hardware trojans into digital circuits. Publications: [WS.2] [WS.3].

ENERGY-RELATED ISSUES

Within the field of energy feasibility analysis of embedded systems, Luca Maria Cassano is working on the evaluation of the energy feasibility of both wireless sensor networks (WSNs) and automatic weather stations (AWSs). A simulator of WSNs has been developed and then used to evaluate the effectiveness of Adaptive-BMAC+, a previously designed energy-aware adaptive MAC protocol. Further, Luca Maria Cassano participated at the design and development of AENEAS: an energy-aware simulator of AWSs. AENEAS was meant to support the designer in the study of the energy behaviour of the system before a prototype is available for energy analysis on the field. The main feature of AENEAS is the ability to perform an holistic simulation of the system under analysis, taking into account the effects on the energy behaviour of both a large variety of hardware components (batteries, microcontrollers, solar panels, wind turbines) and of the software tasks run by the AWS microcontroller. Publications: [JR.8] [JR.5] [IB.1] [IC.3] [IC.10] [IC.12].

COLLABORATIONS

- prof. M. Porrmann of the University of Bielefeld, prof. C. Bernardeschi of the University of Pisa and prof. L. Sterpone of the Politecnico di Torino on the design and development of a self-testing and self-healing processing platform based on reconfigurable computing.
- prof. M. Angel Aguirre and doc. H. Guzman-Miranda of University of Sevilla on the analysis of the untestability of SEU faults in VLSI systems.
- doc. G. Di Natale and doc. A. Bosio of the Laboratoire d'Informatique, de Robotique et de Microlectronique de Montpellier on the design of an adaptive flip-flop architecture for hardware systems having dynamically changing reliability requirements.
- prof. M. Avvenuti of the University of Pisa, doc. D. Cesarini of the Scuola Superiore Sant'Anna and Prof. V. Bilas and Doc. M. Kuri of the University of Zagreb on the design and development of an energy-aware simulator of automatic weather stations.
- prof. R. Saletti, prof. R. Roncella, prof. C. Bernardeschi, doc. A. Domenici and doc. F. Baronti of the University of Pisa on the design and formal verification of the safety driver of a battery management system for Li-ion batteries.
- prof. L. Sterpone of the Politecnico di Torino on the development of an accurate fault simulator for SRAM-based FPGA-based systems.
- prof. M. Avvenuti, prof. C. Bernardeschi and doc. A. Vecchio of the University of Pisa on the performance evaluation of an adaptive MAC protocol for wireless sensor networks.

Professional Activities

National and International Research Projects

Luca Maria Cassano is/has been directly responsible for the following funded research projects:

- *OLTRE: On-Line Testing and Healing Permanent Radiation Effects in Reconfigurable Systems*, an European Space Agency ITI project, 50,000, ESA Contract ITT AO/1-6067/09/NL/CBI (Reference Number: A00016022), running from Jan. 2015 till Sept. 2015. (Work Package 4 "Fault Injection Experimental Evaluation" coordinator: Luca Maria Cassano, Local co-principal investigator: Luca Maria Cassano, project leader: prof. Mario Porrmann)

Luca Maria Cassano also contributes/contributed actively in funded research projects, more precisely:

- *FIND^2: A flexible functional diagnosis framework based on machine-learning techniques*. Cisco University Research Program Fund Gift #2014-130689 (3696). 100,000US$. (Principal investigator: prof. C. Bolchini)
- *Exploiting (historical) test output data to improve functional diagnosis*. Cisco University Research Program Fund Gift #2012-101762 (3696). (Principal investigator: prof. C. Bolchini)
- *TRACE-IT - Train Control Enhancement via Information Technology*, Tuscany Regional Research Project (TRACE-IT, PAR-FAS-2007-2013). (Local principal investigator: doc. S. Gnesi)

Editorial Board Memberships

- Associate Editor of IEEE Access (2018).
- Associate Editor of Integration, the VLSI Journal (2018).
- Associate Editor of Ad Hoc & Sensor Wireless Networks (2018).
- Associate Editor of Simulation (2018).
- Associate Editor of The International Journal of Electrical and Computer Engineering (2018).
- Associate Editor (within the Circuits and Systems subject area) of The Journal of Electrical and Computer Engineering (2018).
- Associate Editor of The International Journal of Electronic Security and Digital Forensics (2018).
- Deputy Section Editor (within the Computing and Software Section) of The Journal of Engineering (2018).

Technical Program Committee Memberships

- The T4 "System-Level Reliability Design, Analysis and On-line Test" track of the Design, Automation and Test in Europe Conference (2019).
- The IEEE European Test Symposium (2015 – present).
- The IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (2018).
- The IEEE International Symposium on On-Line Testing and Robust System Design (2018).
- The ACM Great Lakes Symposium on VLSI (2018).

- The Dependability, Testing, and Fault Tolerance in Digital Systems Session within the Euromicro Conference on Digital System Design (2018).
- The Architecture and Hardware for Security Applications Session within the Euromicro Conference on Digital System Design (2018).
- The IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (2014).
- The Hipeac Workshop on Reconfigurable Computing (2014 – present).
- The Symposium on Modelling and Simulation in Computer Sciences and Engineering (2015)

REFEREE SERVICES

Luca Maria Cassano is a reviewer for several journals and conferences in the field of Computer Aided Design and embedded systems: IEEE Trans. on Computers, IEEE Trans. on VLSI, IEEE Trans. on CAD, IEEE Trans. on Emerging Topics in Computing, IEEE Access, Elsevier International Journal on Microprocessors and Microsystems, ICCAD, ICIT, IOLTS, DFTS, ARC and ARCS.

Teaching activity

2017 – Ongoing

Fundamental of Computer Science (*Teacher*) - Mechanical and Energetic Engineering - Undergraduate level, Politecnico di Milano. 7 CFU (35 hours lecturer + 10 hours teaching assistant)

2013 – 2016

Fundamental of Computer Science (*Lab. supervisor*) - Computer Engineering - Undergraduate level, Politecnico di Milano. 10 CFU (18 hours laboratory supervisor)

2010 – 2013

Fundamental of Computer Science (*Lab. supervisor*) - Computer Engineering - Undergraduate level, University of Pisa. 12 CFU (18 hours laboratory supervisor)

STUDENTS' SUPERVISION

Graduate Students Supervision/Co-Advisor

- *Filippo Mascolo*, 2015, "Design and implementation of a routing algorithm to maximize test coverage of permanent faults in FPGAs". Unibersity of Pisa.
- *Luca Santangelo*, 2014, "Viv2XDL: a bridge between Vivado and XDL based software". University of Pisa.
- *Domenico Sorrenti*, 2014, "Exploiting Partial Dynamic Reconfiguration for On-Line On-Demand Detection of Permanent Faults in SRAM-based FPGAs". University of Pisa.
- *Alessio Fagioli*, 2013, "Modeling and Simulation of Automatic Weather Stations with mixed energy sources for the design of Sensing and Communication policies". University of Pisa.
- *Silvia Mandalá*, 2013, "Verso l'autonomic sensing: simulazione e valutazione energetica di una Automatic Weather Station". University of Pisa.
- *Alessio Amato*, 2011, "Simulazione e valutazione di un protocollo MAC adattivo per reti di sensori tramite Stochastic Activity Networks". University of Pisa.
- *Massimiliano Leone Itria*, 2011, "Progetto e realizzazione di un traduttore per il linguaggio EDIF orientato a sistemi FPGA". University of Pisa.

Selected publications[1]

These are the 5 selected publications.

1. D. Cozzi, S. Korf, L. Cassano, J. Hagemeyer, A. Domenici, C. Bernardeschi, M. Porrmann and L. Sterpone, "OLT(RE)^2: an On-Line on-demand Testing approach for permanent Radiation Effects in REcongurable systems", To appear in *IEEE Trans. on Emerging Topics in Computing*

   [doi: http://dx.doi.org/10.1109/TC.2015.2417537]

2. C. Bolchini and L. Cassano, "A Novel Approach to Incremental Functional Diagnosis for Complex Electronic Boards," *IEEE Transactions on Computers* Vol. 65, no. 1, (2016), pp. 42-52, (ISSN: 0018-9340)

   [doi: http://dx.doi.org/10.1109/TC.2015.2417537]

3. C. Bolchini, L. Cassano, P. Garza, E. Quintarelli, and F. Salice, "An Expert CAD Flow for Incremental Functional Diagnosis of Complex Electronic Boards," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Vol. 34, no. 5, (2015), pp. 835-848, (ISSN: 0278-0070)

   [doi: http://dx.doi.org/10.1109/TCAD.2015.2396997]

4. C. Bernardeschi, L. Cassano, A. Domenici, and L. Sterpone, "ASSESS: A Simulator of Soft Errors in the Configuration Memory of SRAM-based FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Vol. 33, no. 9, (2014), pp. 1342-1355, (ISSN: 0278-0070)

   [doi: http://dx.doi.org/10.1109/TCAD.2014.2329419]

5. F. Baronti, C. Bernardeschi, L. Cassano, A. Domenici, R. Roncella, R. Saletti, "Design and Safety Verification of a Distributed Charge Equalizer for Modular Li-ion Batteries," *IEEE Transactions on Industrial Informatics* Vol. 10, no. 2, (2014), pp. 1003-1011, (ISSN: 1551-3203)

   [doi: http://dx.doi.org/10.1109/TII.2014.2299236]

Complete publication list

PUBLICATION LIST

h-index: 8 ◇ Total citations: 198 ◇ Academic age: 8 years (src: Google Scholar, May 2018).
h-index: 7 ◇ Total citations: 140 ◇ Academic age: 8 years (src: Scopus, May 2018).

[1] In Italy, authors typically appear in alphabetical order

REFEREED INTERNATIONAL JOURNALS

JR.1. D. Cozzi, S. Korf, L. Cassano, J. Hagemeyer, A. Domenici, C. Bernardeschi, M. Porrmann and L. Sterpone, "OLT(RE)^2: an On-Line on-demand Testing approach for permanent Radiation Effects in REcongurable systems", To appear in *IEEE Trans. on Emerging Topics in Computing*

[doi: http://dx.doi.org/10.1109/TC.2015.2417537]

JR.2. C. Bolchini and L. Cassano, "A Fully Automated and Congurable Cost-Aware Framework for Adaptive Functional Diagnosis", *IEEE Design & Test*, Vol. 34, no. 2, (2017), pp. 79-86

[doi: http://dx.doi.org/10.1109/MDAT.2016.2550584]

JR.3. C. Bernardeschi, L. Cassano, A. Domenici and L. Sterpone, UA^{2}TPG: "An untestability analyzer and test pattern generator for SEUs in the configuration memory of SRAM-based FPGAs," *Integration, the VLSI Journal* vol. 55 (2016), pp. 85-97 [doi: http://dx.doi.org/10.1016/j.vlsi.2016.03.004]

JR.4. C. Bolchini and L. Cassano, "A Novel Approach to Incremental Functional Diagnosis for Complex Electronic Boards," *IEEE Transactions on Computers* Vol. 65, no. 1, (2016), pp. 42-52, (ISSN: 0018-9340)

[doi: http://dx.doi.org/10.1109/TC.2015.2417537]

JR.5. M. Avvenuti, C. Bernardeschi, L. Cassano, and A. Vecchio, "Adapting the duty cycle to traffic load in a preamble sampling MAC for WSNs," *Ad Hoc & Sensor Wireless Networks* Vol. 31, no. 1-4, (2016), pp. 101-129, (ISSN: 1552-0633)

JR.6. C. Bernardeschi, L. Cassano, and A. Domenici, "SRAM-based FPGA Systems for Safety-Critical Applications: A Survey on Design Standards and Proposed Methodologies," *Journal of Computer Science and Technology* Vol. 30, no. 2, (2015), pp. 373-390, (ISSN: 1000-9000), (ISSN: 1860-4749)

[doi: http://dx.doi.org/10.1007/s11390-015-1530-5]

JR.7. C. Bolchini, L. Cassano, P. Garza, E. Quintarelli, and F. Salice, "An Expert CAD Flow for Incremental Functional Diagnosis of Complex Electronic Boards," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Vol. 34, no. 5, (2015), pp. 835-848, (ISSN: 0278-0070)

[doi: http://dx.doi.org/10.1109/TCAD.2015.2396997]

JR.8. D. Cesarini, L. Cassano, M. Avvenuti, M. Kuri, V. Bilas, "AENEAS: an Energy-Aware Simulator of Automatic Weather Stations," *IEEE Sensors Journal* Vol. 14, no. 11, (2014), pp. 3932-3943, (ISSN: 1530-437X)

[doi: http://dx.doi.org/10.1109/JSEN.2014.2353011]

JR.9. C. Bernardeschi, L. Cassano, A. Domenici, and L. Sterpone, "ASSESS: A Simulator of Soft Errors in the Configuration Memory of SRAM-based FPGAs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Vol. 33, no. 9, (2014), pp. 1342-1355, (ISSN: 0278-0070)

[doi: http://dx.doi.org/10.1109/TCAD.2014.2329419]

JR.10. F. Baronti, C. Bernardeschi, L. Cassano, A. Domenici, R. Roncella, R. Saletti, "Design and Safety Verification of a Distributed Charge Equalizer for Modular Li-ion Batteries," *IEEE Transactions on Industrial Informatics* Vol. 10, no. 2, (2014), pp. 1003-1011, (ISSN: 1551-3203)

[doi: http://dx.doi.org/10.1109/TII.2014.2299236]

JR.11. C. Bernardeschi, L. Cassano, M.G.C.A. Cimino, A. Domenici, "GABES: a Genetic Algorithm Based Environment for SEU Testing in SRAM-FPGAs," *Journal of Systems Architecture* Vol. 59, no. 10, part D, (2013), pp. 1243-1254, (ISSN: 1383-7621)

[doi: http://dx.doi.org/10.1016/j.sysarc.2013.10.006]

JR.12. C. Bernardeschi, L. Cassano, A. Domenici, P. Masci, "Simulation and Test-Case Generation for PVS Specifications of Control Logics," *International Journal On Advances in Software* Vol. 5, no. 1&2, (2011), pp. 327-341, (ISSN: 1942-2628)

REFEREED CHAPTERS IN INTERNATIONAL BOOKS

IB.1. L. Cassano, D. Cesarini, M. Avvenuti, "On the use of Stochastic Activity Networks for an Energy-aware Simulation of Automatic Weather Stations," In *Handbook of Research on Computational Simulation and Modeling in Engineering*, ed. Francisco Miranda and Carlos Abreu, pp. 184-207 (2016)

[doi: http://dx.doi.org/10.4018/978-1-4666-8823-0.ch006]

TUTORIAL

TU.1. L. Cassano, K. Chakrabarty, B. Eklow, " Board-level functional fault diagnosis: industry needs and research solutions ," *DATE 2016, Design Automation & Test in Europe*

REFEREED INTERNATIONAL CONFERENCES/SYMPOSIA/WORKSHOPS WITH FORMAL PROCEEDINGS

IC.1. C. Bolchini, L. Cassano, A. Miele, " Lifetime-aware Load Distribution Policies in Multi-core Systems: An In-depth Analysis," *Proc. DATE 2016, Design Automation & Test in Europe*, Dresden, Germany, March 14-18, 2016, pp. 1 - 4.

IC.2. C. Bolchini and L. Cassano, "A Configurable Board-level Adaptive Incremental Diagnosis Technique based on Decision Trees," *Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT), University of Massachusetts Amherst, USA, October 12-14, 2015.
[doi: http://dx.doi.org/10.1109/DFT.2015.7315167]

IC.3. L. Cassano, D. Cesarini, M. Avvenuti, "Using Stochastic Activity Networks to Study the Energy Feasibility of Automatic Weather Stations," *Proc. Symposium on Modelling and Simulation in Computer Sciences and Engineering* (MSCSE), Rhodes, Greece, September 22-28, 2014, pp. 1 - 4.
[doi: http://dx.doi.org/10.1063/1.4912935]

IC.4. D. Sorrenti, D. Cozzi, S. Korf, L. Cassano, J. Hagemeyer, M. Porrmann and C. Bernardeschi, "Exploiting Dynamic Partial Reconfiguration for On-Line On-Demand Testing of Permanent Faults in Reconfigurable Systems," *Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT), Amsterdam, The Netherlands, October 1-3, 2014, pp. 203 - 208.
[doi: http://dx.doi.org/10.1109/DFT.2014.6962065]

IC.5. C. Bolchini and L. Cassano, "Machine Learning-based Techniques for Board-level Incremental Functional Diagnosis: a Comparative Analysis," *Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT), Amsterdam, The Netherlands, October 1-3, 2014, pp. 246 - 251.
[doi: http://dx.doi.org/10.1109/DFT.2014.6962064]

IC.6. L. Cassano, "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs," *Proc. IEEE International Test Conference* (ITC), Seattle, Washington, USA, October 21-23, 2014, pp. 1 - 10.
[doi: http://dx.doi.org/10.1109/TEST.2014.7035366]

IC.7. L. Cassano, H. Guzman-Miranda and M.A. Aguirre, "Early Assessment of SEU Sensitivity through Untestable Faults Identification," *Proc. IEEE International On-Line Testing Symposium* (IOLTS), Platja d'Aro, Catalunya, Spain, July 7-9, 2014, pp. 186 - 189.
[doi: http://dx.doi.org/10.1109/IOLTS.2014.6873692]

IC.8. L. Cassano, D. Cozzi, D. Jungewelter, S. Korf, J. Hagemeyer, M. Porrmann and C. Bernardeschi, "An Inter-Processor Communication Interface for Data-Flow Centric Heterogeneous Embedded Multiprocessor Systems," *Proc. IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era* (DTIS), Santorini, Greece, May 6-8, 2014, pp. 1 - 6.
[doi: http://dx.doi.org/10.1109/DTIS.2014.6850669]

IC.9. L. Cassano, A. Bosio and G. Di Natale, "A novel Adaptive Fault Tolerant Flip-Flop Architecture based on TMR," *Proc. IEEE European Test Symposium* (ETS), Paderborn, Germany, May 26-30, 2014, pp. 1 - 2.
[doi: http://dx.doi.org/10.1109/ETS.2014.6847831]

IC.10. D. Cesarini, L. Cassano, A. Fagioli and M. Avvenuti, "Modeling and Simulation of Energy-Aware Adaptive Policies for Automatic Weather Stations," *Proc. DATE 2014 Workshop on Engineering Simulations for Cyber-Physical Systems* (ES4CPS), Bremen, Germany, March 28, 2014, pp. 44 - 47.
[doi: http://dx.doi.org/10.1145/2559627.2559631]

IC.11. F. Baronti, C. Bernardeschi, L. Cassano, A. Domenici, R. Roncella, R. Saletti, "Mitigation of Single Event Upsets in the Control Logic of a Charge Equalizer for Li-ion Batteries," *Proc. Annual Conference of the IEEE Industrial Electronics Society* (IECON), Vienna, Austria, November 10-13, 2013, pp. 6758 - 6763.
[doi: http://dx.doi.org/10.1109/IECON.2013.6700251]

IC.12. M. Avvenuti, L. Cassano, D. Cesarini and S. Mandalá, "Simulation of Automatic Weather Stations for the Energy Estimation of Sensing and Communication Software Policies," *Proc. Extreme Conference on Communication* (ExtremeCom), Iceland, August 24-30, 2013, pp. 1 - 6.

IC.13. C. Bernardeschi, L. Cassano and A. Domenici, "Formal approaches to SEU testing in FPGAs," *Proc. NASA/ESA Conference on Adaptive Hardware and Systems* (AHS), Torino, Italy, June 25-27, 2013, pp. 209 - 216.
[doi: http://dx.doi.org/10.1109/AHS.2013.6604248]

IC.14. C. Bernardeschi, L. Cassano, A. Domenici and L. Sterpone, "Unexcitability Analysis of SEUs Affecting the Routing Structure of SRAM-based FPGAs," *Proc. Great Lakes Symposium on Very Large Scale of Integration* (GLSVLSI), Paris, France, May 2-3, 2013, pp. 7 - 12.
[doi: http://dx.doi.org/10.1145/2483028.2483050]

IC.15. L. Cassano, D. Cozzi, S. Korf, J. Hagemeyer, M. Porrmann and L. Sterpone, "On-Line Testing of Permanent Radiation Effects in Reconfigurable Systems," *Proc. Design Automation & Test in Europe* (DATE), Grenoble, France, March 18-22, 2013, pp. 717 - 720.
[doi: http://dx.doi.org/10.7873/DATE.2013.154]

IC.16. C. Bernardeschi, L. Cassano, A. Domenici, L. Sterpone, "Accurate Simulation of SEUs in the Configuration Memory of SRAM-based FPGAs," *Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems* (DFT), Austin, Texas, USA, October 3-5, 2012, pp. 115 - 120.
[doi: http://dx.doi.org/10.1109/DFT.2012.6378210]

IC.17. C. Bernardeschi, L. Cassano, A. Domenici, "SEU-X: a SEu Un-eXcitability prover for SRAM-FPGAs," *Proc. IEEE International On-Line Testing Symposium* (IOLTS), Sitges, Spain, June 27-29, 2012, pp. 25 - 30.
[doi: http://dx.doi.org/10.1109/IOLTS.2012.6313836]

IC.18. C. Bernardeschi, L. Cassano, A. Domenici, G. Gennaro, M. Pasquariello, "Simulated Injection of Radiation-Induced Logic Faults in FPGAs," *Proc. International Conference on Advances in System Testing and Validation Lifecycle* (VALID), SBarcelona, Spain, October 23-28, 2011, pp. 84 - 89.

IC.19. C. Bernardeschi, L. Cassano, A. Domenici, P. Masci, "A Tool for Signal Probability Analysis of FPGA-Based Systems," *Proc. International Conference on Computational Logics, Algebras, Programming, Tools, and Benchmarking* (COMPUTATION TOOLS), Rome, Italy, September 25-30, 2011, pp. 13 - 18,.

IC.20. C. Bernardeschi, L. Cassano, A. Domenici, "Failure Probability and Fault Observability of SRAM-FPGA Systems," *Proc. International Conference on Field Programmable Logic and Applications* (FPL), Chania, Crete, Greece, September 5-7, 2011, pp. 385 - 388.
[doi: http://dx.doi.org/10.1109/FPL.2011.75]

IC.21. C. Bernardeschi, L. Cassano, A. Domenici, "Failure Probability of SRAM-FPGA Systems with Stochastic Activity Networks," *Proc. IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems* (DDECS), Cottbus, Germany, April 13-15, 2011, pp. 293 - 296.
[doi: http://dx.doi.org/10.1109/DDECS.2011.5783098]

IC.22. C. Bernardeschi, L. Cassano, A. Domenici, P. Masci, "Debugging PVS Specifications of Control Logics via Event-driven Simulation," *Proc. International Conference on Computational Logics, Algebras, Programming, Tools, and Benchmarking* (COMPUTATION TOOLS), Lisbon, Portugal, November 21-26, 2010, pp. 1 - 7.

REFEREED INTERNATIONAL WORKSHOPS AND POSTER PRESENTATIONS WITHOUT FORMAL PROCEEDINGS

WS.1. C. Bolchini, L. Cassano, "Reducing the Effort for Board-level Functional Diagnosis through Incremental Test Execution," *International Test Conference* (ITC), Seattle, Washington, USA, October 21-23, 2014.

WS.2. C. Bolchini, L. Cassano, G. Di Natale, "Multi-stage Cross-layer Hardware Trojan Prevention, Detection and Tolerance," *Joint MEDIAN-TRUDEVICE Open Forum*, Amsterdam, The Netherlands, September 30, 2014.

WS.3. C. Bolchini, L. Cassano,, "Detecting Possible Locations for Hardware Trojans by Identifying Untestable Faults," *Workshop on Test and Fault Tolerance for Secure Devices* (TRUDEVICE), Paderborn, Germany, May 29-30, 2014.

WS.4. L. Cassano, "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs," *E.J. McCluskey Doctoral Thesis Award Semifinals*, Paderborn, Germany, May 26-30, 2014.

WS.5. L. Cassano, "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs," *EDAA/ACM SIGDA PhD Forum at DATE 2014*, Bremen, Germany, March 24-28, 2014.

WS.6. L. Cassano, D. Cozzi, S. Korf, J. Hagemeyer, M. Porrmann and L. Sterpone, "A CAD Flow for On-Line Testing and Patching Permanent Radiation Effects in Reconfigurable Systems," *SEE/MAPLD 2013 joint session of the Single Event Effects Symposium and Military and Aerospace Programmable Logic Devices Conference*, San Diego, California, USA, April 9-12, 2013.

WS.7. L. Cassano, "A CAD Flow for the Analysis of the Sensitivity to SEUs of SRAM-FPGAs," *ESA SpacE FPGA Users Workshop* (SEFUW), Nordwjik, The Netherlands, November 6-7, 2012.

WS.8. C. Bernardeschi, L. Cassano, M.G.C.A. Cimino, A. Domenici, "Application of a Genetic Algorithm for Testing SEUs in SRAM-FPGA Systems," *HiPEAC Workshop on Reconfigurable Computing* (WRC), Paris, France, January 24, 2012.

INVITED TALKS AND SEMINARS

IN.1. "Analysis and Test of the Effects of Single Event Upsets in the Configuration Memory of SRAM-based FPGA Systems," held at *Istituto di Scienza e Tecnologie dellInformazione A. Faedo - National Research Council of Italy (CNR)*, Pisa, Italy, March 1, 2013.

IN.2. "Reconfigurable Systems: the Dynamically Reconfigurable Processing Module Project," held at *Department of Information Engineering, University of Pisa*, Italy, October 22, 2012.

IN.3. "Tools for the Analysis of SEU Effects into SRAM-FPGA Systems," held at *Cluster of Excellence Center in Cognitive Interactive Technology (CITEC) - University of Bielefeld*, Germany, April 20, 2012.

IN.4. "An Introduction to Fault Detection in FPGA Systems," held at *Department of Information Engineering, University of Pisa*, Italy, January 31, 2012.

AWARDS

AW.1. Winner of the European semi-finals of the 2014 TTTC's E. J. McCluskey Doctoral Thesis Award with the PhD thesis "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs,".

AW.2. Runner-up of the Finals of the 2014 TTTC's E. J. McCluskey Doctoral Thesis Award with the PhD thesis "Analysis and Test of the Effects of Single Event Upsets Affecting the Configuration Memory of SRAM-based FPGAs,".